1MHz 3A, Synchronous Step-Down Regulator

General Description

EML3505 is a high efficiency step down DC/DC converter. It features an extremely low quiescent current, which is suitable for reducing standby power consumption, especially for portable applications.

The device can accept input voltage from 2.5V to 5.5V and deliver up to 3A output current. The high switching frequency (1MHz) of the converter allows the use of small surface mount inductors and capacitors to reduce overall PCB board space. Furthermore, the built-in synchronous switch improves efficiency and eliminates external Schottky diode. EML3505 uses different modulation algorithms for various loading conditions: (1) Pulse Width Modulation (PWM) for low output voltage ripple and fixed frequency noise, (2) Pulse Frequency Modulation (PFM) for improving light load efficiency, and (3) Low Dropout (LDO) Mode for providing 100% duty cycle operation during heavy loading. Adopting low reference voltage design reduces regulated output to 0.6V. The adjustable version of this device is available in TDFN package.

Features

- Achieve 97% efficiency
- Input voltage : 2.5V to 5.5V
- Output current up to 3A
- Reference voltage: 0.6V
- Quiescent current 25μA with no load
- Internal switching frequency: 1MHz
- No Schottky diode needed
- Low dropout operation: 100% duty cycle
- Shutdown current < 1μA
- Excellent line and load transient response
- Over temperature protection
- Over voltage protection (112% of V_{FB})

Applications

- Blue-Tooth devices
- Cellular and Smart Phones
- Personal Multi-media Player (PMP)
- Wireless networking
- Digital Still Cameras
- Portable applications

Typical Application

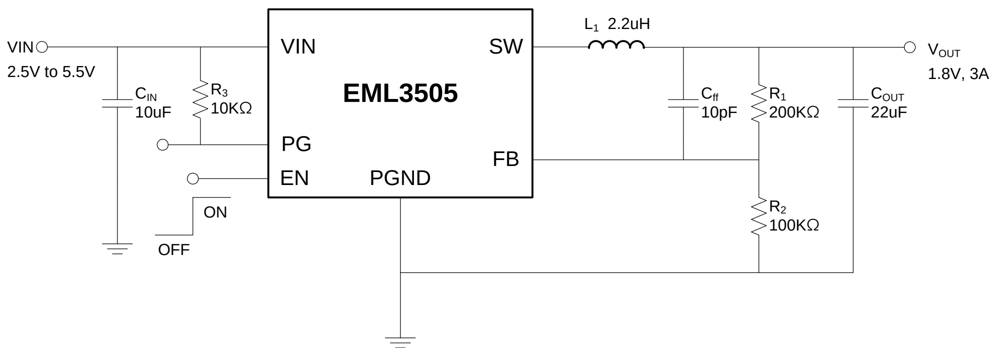
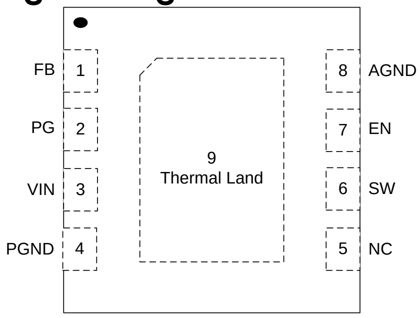


Fig. 1

Package Configuration

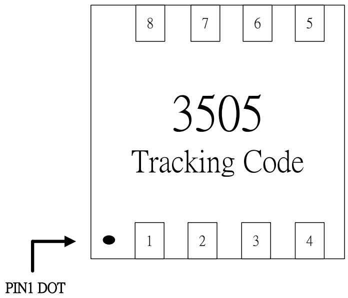


TDFN-8L (2mm*2mm)

EML3505-00FK08NRR

00	Adjustable
FK08	TDFN-8L Package
NRR	RoHS & Halogen free package Commercial Grade Temperature Rating: -40 to 85°C Package in Tape & Reel

Order, Mark & Packing information

Package	Vout(V)	Product ID	Marking	Packing
TDFN-8L	adjustable	EML3505-00FK08NRR		Tape & Reel 3K units

Pin Functions

Pin Name	TDFN-8L	Function
FB	**1**	**Feedback Pin.** Receives the feedback voltage from an external resistive divider across the output.
PG	**2**	**Power Good Indicator.** The output of this pin is an open-drain. If the output is within 90% of regulation, It's low otherwise.
VIN	**3**	**Power Input Pin.** Must be closely decoupled to GND pin with a 10μF or greater ceramic capacitor.
PGND	**4**	**Power Ground Pin.**
NC	**5**	**N.C.**
SW	**6**	**Switch Pin.** Must be connected to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.
EN	**7**	**Enable Pin.** Minimum 1.5V to enable the device. Maximum 0.5V to shut down the device.
AGND	**8**	**Analog Ground Pin.**
Thermal Land	**9**	**Connected it to GND.**

Absolute Maximum Ratings

Devices are subjected to fail if they stay above absolute maximum ratings.

Input Voltage -- – 0.3V to 6V
EN, VFB Voltages ----------------------------------- – 0.3V to V_{IN}
SW(DC) Voltage ------------------------ – 0.3V to (V_{IN} + 0.3V)
SW(AC, less than 20ns) Voltage ----------------- – 3V to 7.5V
Lead Temperature (Soldering, 10 sec)---------------- 260°C

Operating Temperature Range ---------- –40°C to 85°C
Junction Temperature (Notes 1, 2) -------------------- 150°C
Storage Temperature Range ------------- – 65°C to 150°C
ESD Susceptibility HBM ------------------------------------ 2000V
CDM --------------------------------------- 500V

Recommended Operating Conditions

Input Voltage (V_{IN}) ------------------------------- +2.5V to +5.5V

Junction Operating Temperature --------- –40°C to 125°C

Thermal data

Package	Thermal resistance	Parameter	Value
TDFN-8L (2mmx2mm)	θ_{JA} (Note 3)	Junction-ambient	74.7°C /W
	θ_{JC} (Note 4)	Junction-case	24°C /W

Electrical Characteristics

V_{IN} = 3.6V, T_A = 25°C, unless otherwise specified.

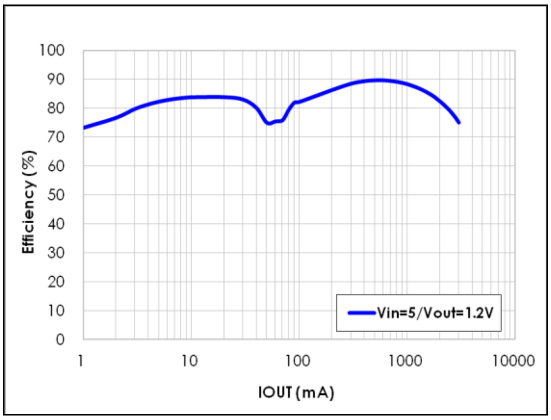
Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage Range		2.5		5.5	V
I_{VFB}	Feedback Current				±100	nA
V_{FB}	Regulated Feedback Voltage		0.588	0.600	0.612	V
V_{OUT}%	Output Voltage Accuracy	I_{OUT}=100mA	-3		+3	%
ΔV_{FB}	Reference Voltage Line Regulation	V_{IN} = 2.5V to 5.5V			0.4	%/V
I_{PK}	Peak Inductor Current (Note 5)	V_{FB} = 0.5V or V_{OUT} = 90%,	3			A
I_Q	PWM Quiescent Current	V_{FB} = 0.5V or V_{OUT} = 90%		256		μA
	PFM Quiescent Current	V_{FB} = 0.65V or V_{OUT} = 108%		25		μA
	Shutdown	V_{EN} = 0V		0.1	1	μA
f_{OSC}	Oscillator Frequency	V_{FB} = 0.6V or V_{OUT} = 100%		1.0		MHz
	Short-Circuit Oscillator Frequency	V_{FB} = 0V or V_{OUT} = 0V		500		kHz
R_{PFET}	$R_{DS(ON)}$ of PMOS	I_{SW} = 100mA		105		mΩ
R_{NFET}	$R_{DS(ON)}$ of NMOS	I_{SW} = –100mA		69		mΩ
V_{UVLO}	VIN UVLO Threshold	Wake up		2.2		V
	VIN UVLO Hysteresis			0.4		V
V_{EN}	Enable Threshold		1.5			V
	Shutdown Threshold				0.5	V
I_{EN}	EN Leakage Current				±1	μA
T_{SD}	Thermal Shutdown			150		℃
	Thermal Shutdown Hysteresis			15		℃

Note 1: T_J is a function of the ambient temperature T_A and power dissipation P_D ($T_J = T_A + (P_D)$ * (134.5°C/W)).
Note 2: This IC has a built-in over-temperature protection to avoid damage from overloaded conditions.
Note 3: θ_{JA} is measured in the natural convection at T_A=25℃ on a highly effective thermal conductivity test board (2 layers , 2S0P) according to the JEDEC 51-7 thermal measurement standard.
Note 4: θ_{JC} represents the heat resistance between the chip and the package top case.
Note 5: Design guaranteed.

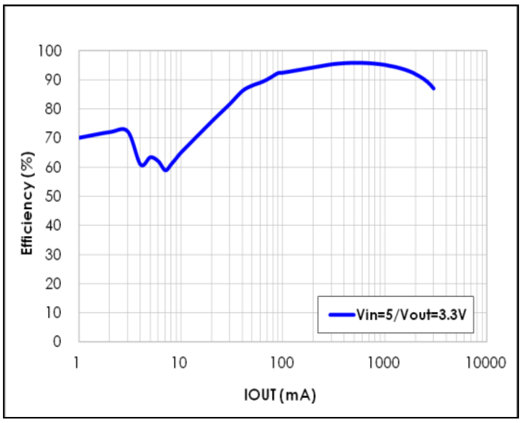
Typical Performance Characteristics

V_{IN}=5V, V_{OUT}=1.2V, C_{IN}=10uF, C_{OUT}=22uF*2, L=1.5uH, T_A=25℃, unless otherwise specified

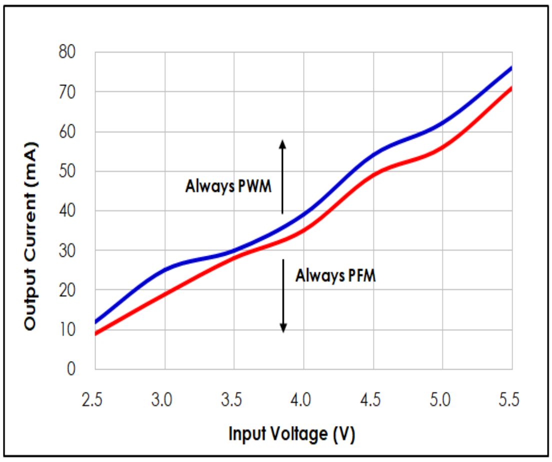
Efficiency vs. Output Current (V_{OUT}=1.2V)



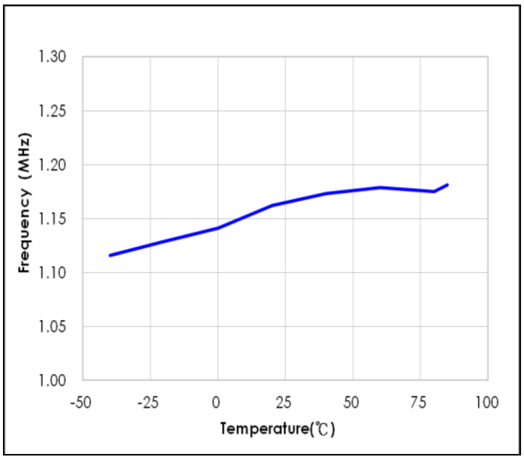
Efficiency vs. Output Current (V_{OUT}=3.3V)



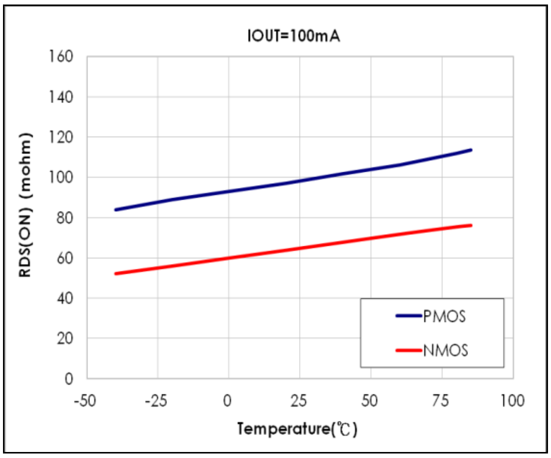
PFM/PWM Boundaries (V_{OUT}=1.2V)



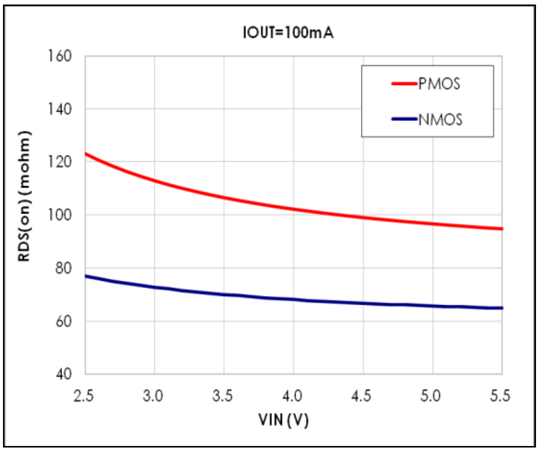
Oscillator Frequency vs. Temperature



$R_{DS(ON)}$ vs. Temperature



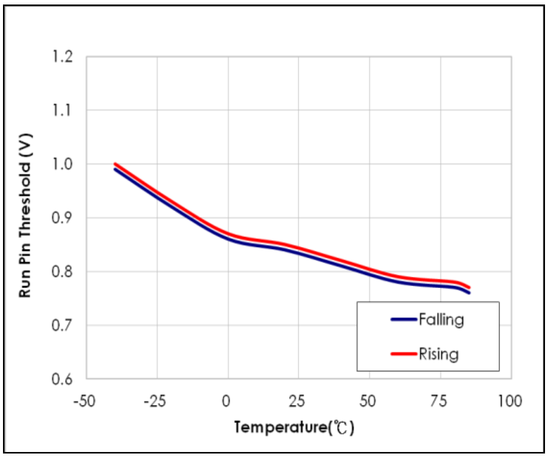
$R_{DS(ON)}$ vs. Input Voltage



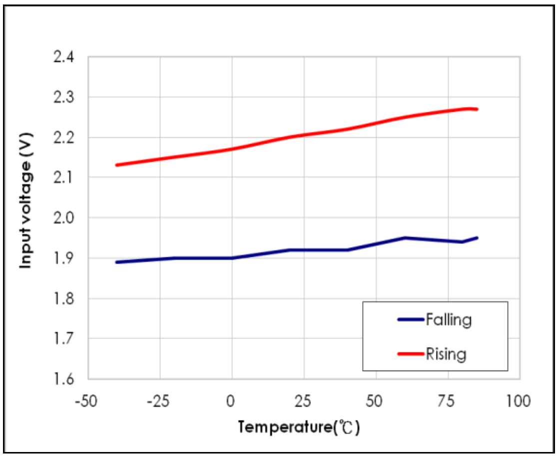
Typical Performance Characteristics (cont.)

V_{IN}=5V, V_{OUT}=1.2V, C_{IN}=10uF, C_{OUT}=22uF*2, L=1.5uH, T_A=25℃, unless otherwise specified

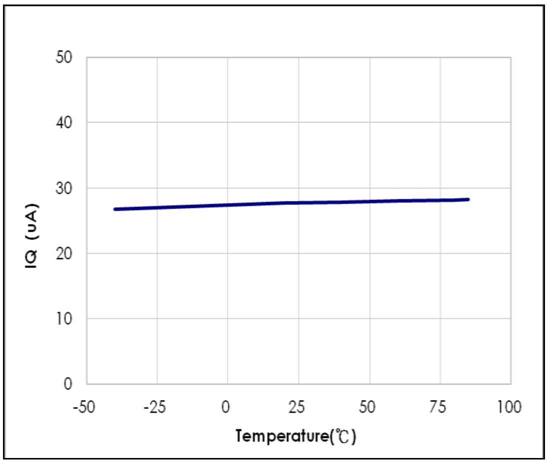
EN Pin Threshold vs. Temperature



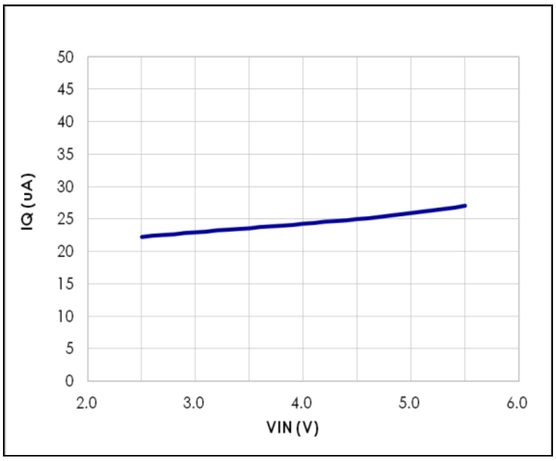
UVLO Threshold vs. Temperature



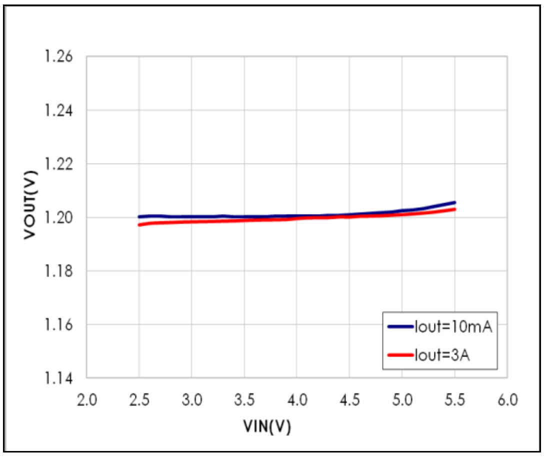
Quiescent Current vs. Temperature (PFM Mode)



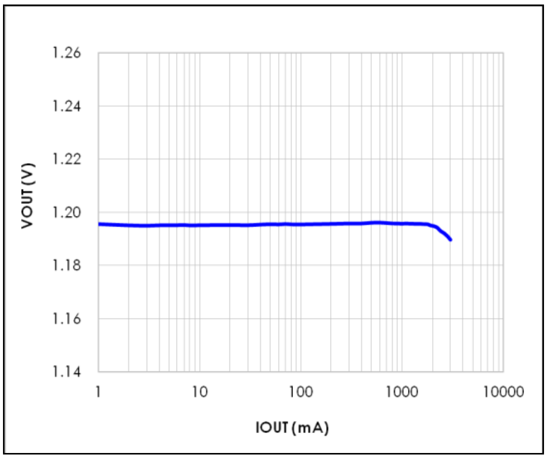
Quiescent Current vs. Input Voltage (PFM Mode)



Line Regulation



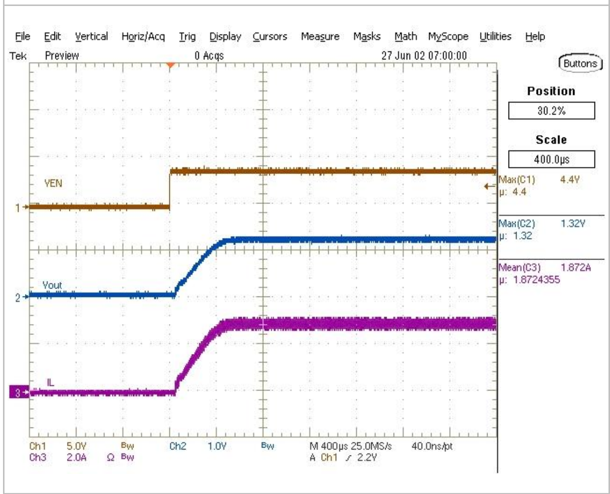
Load Regulation



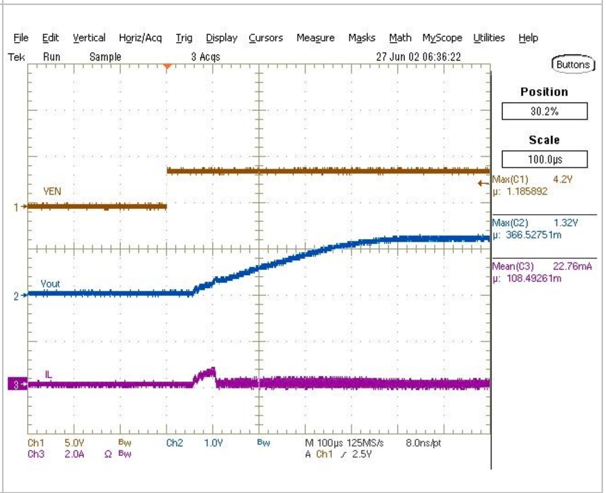
Typical Performance Characteristics (cont.)

V_{IN}=5V, V_{OUT}=1.2V, C_{IN}=10uF, C_{OUT}=22uF*2, L=1.5uH, T_A=25℃, unless otherwise specified

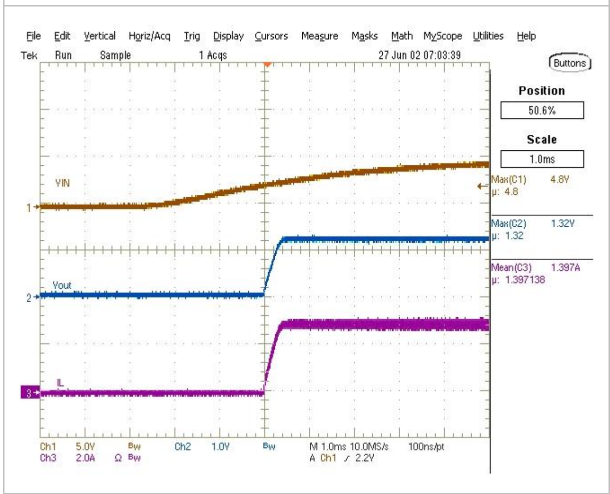
Power-On from EN Pin (I_{OUT}=3A)



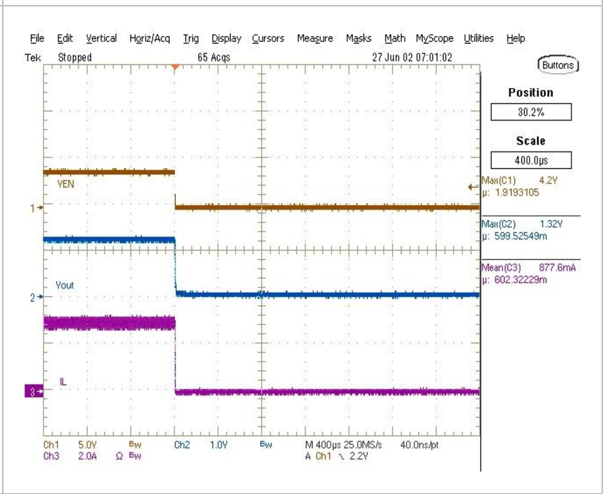
Power-On from EN Pin (I_{OUT}=10mA)



Power-On from VIN (I_{OUT}=3A)

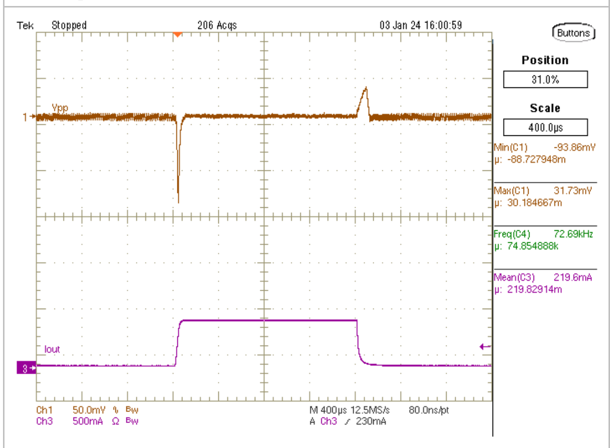


Power-Off from EN Pin (I_{OUT}=3A)



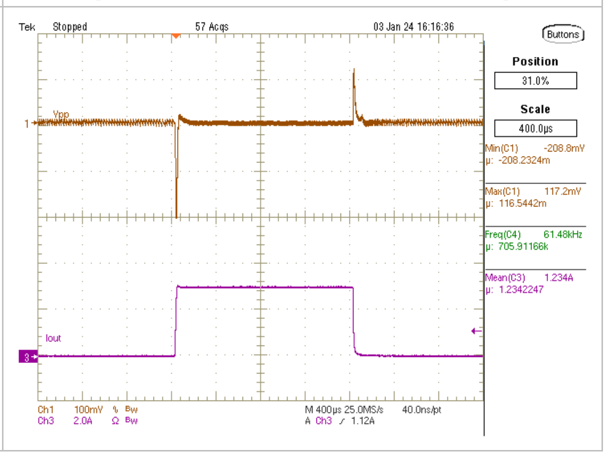
Load Step Response

(V_{OUT}=1.2V, I_{OUT} from 10mA to 500mA



Load Step Response

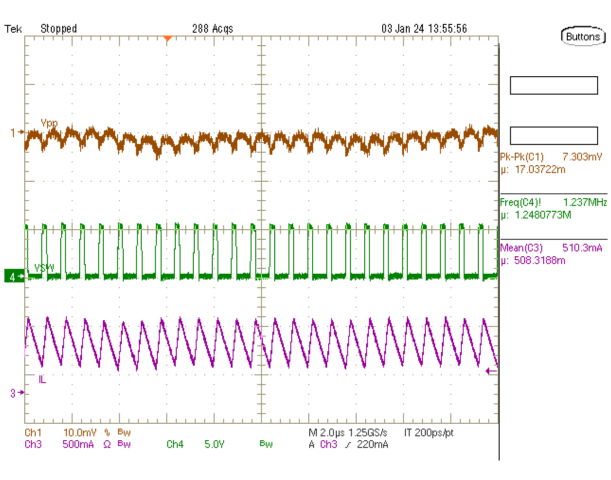
(V_{OUT}=1.2V, I_{OUT} from 10mA to 3A)



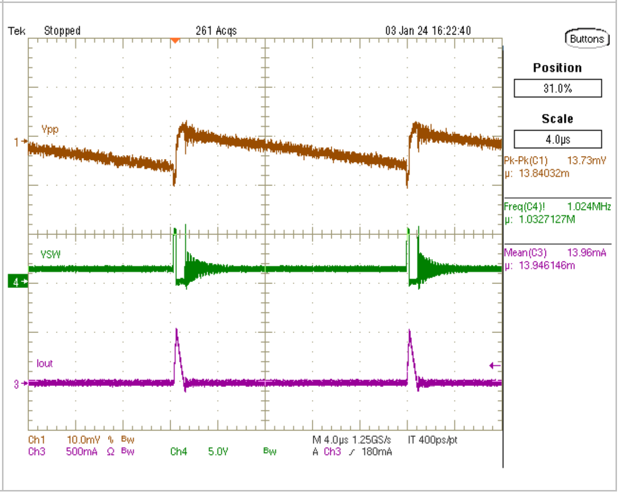
Typical Performance Characteristics (cont.)

V_{IN}=5V, V_{OUT}=1.2V, C_{IN}=10uF, C_{OUT}=22uF*2, L=1.5uH, T_A=25℃, unless otherwise specified

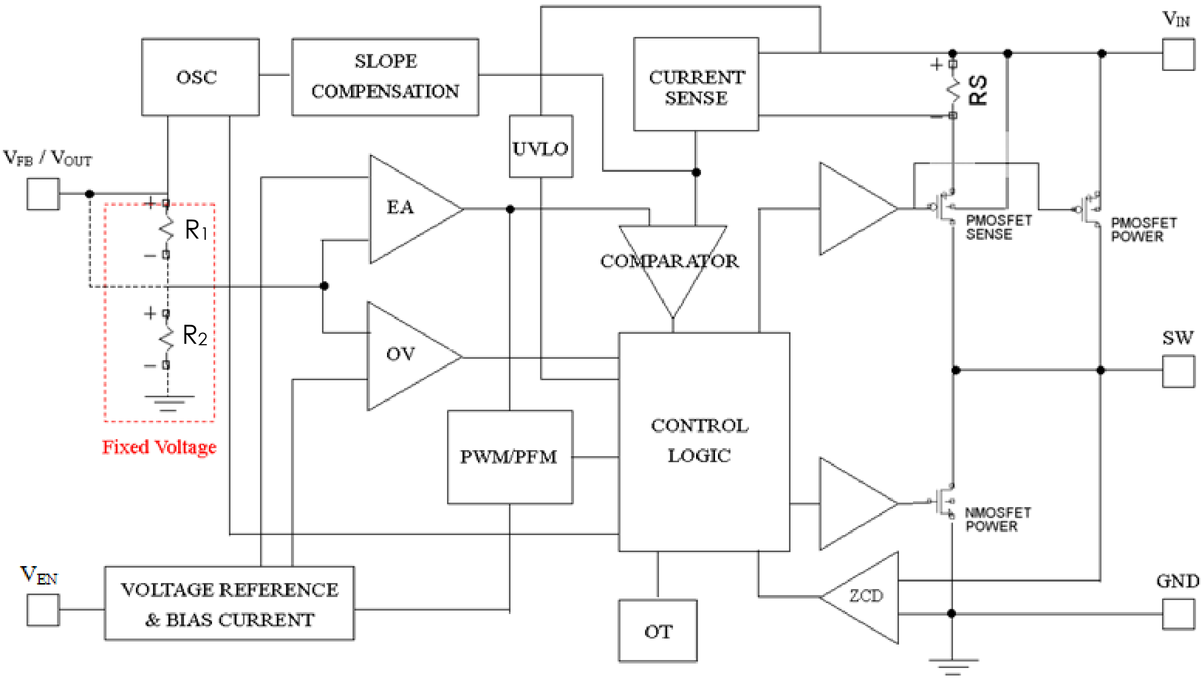
PWM Output Ripple Voltage (I_{OUT}=0.5A)



PFM Output Ripple Voltage (I_{OUT}=10mA)



Functional Block Diagram



Applications

The typical application circuit of adjustable version is shown in Fig.1.

Inductor Selection

Inductor ripple current and core saturation current are the two main factors that decide the Inductor value. A low DCR inductor is preferred.

C_{IN} and C_{OUT} Selection

A low ESR input capacitor can prevent large voltage transients at V_{IN}. The RMS current of input capacitor is required larger than I_{RMS} calculated by:

$$I_{RMS} \cong I_{OMAX}\frac{\sqrt{V_{OUT}(V_{IN}-V_{OUT})}}{V_{IN}} \qquad \text{Eq. 1}$$

ESR is an important parameter to select C_{OUT}, which can be seen in the following output ripple V_{OUT} equation:

$$\Delta V_{OUT} \cong \Delta I_L\left(ESR+\frac{1}{8\cdot f\cdot C_{OUT}}\right) \qquad \text{Eq. 2}$$

Cheaper and smaller ceramic capacitors with higher capacitance values are now commercially available. These ceramic capacitors have low ripple currents, high voltage ratings and low ESR which make them suitable for switching regulator applications. It is feasible to optimize very low output ripples by C_{OUT} since C_{OUT} does not affect the internal control loop stability. X5R or X7R types are recommended since they have the best temperature and voltage characteristics of all ceramics capacitors.

Output Voltage (EML3505 adjustable)

In the adjustable version, the output voltage can be determined by:

$$V_{OUT} = 0.6V\left(1+\frac{R_1}{R_2}\right) \qquad \text{Eq. 3}$$

V_{OUT}(V)	R_1(KΩ)	R_2(KΩ)	C_{OUT}(μF)	C_{ff}(pF)	L(μH)
1.2	100	100	22x2	22	1.5
1.8	200	100	22	10	2.2
3.3	450	100	22	5	2.2

Table.1- Recommended Component Selection

Thermal Considerations

Although the thermal shutdown circuit is designed in EML3505 to protect the device from thermal damage, the total power dissipation that EML3505 can sustain depends on the thermal capability of the package. The formula to ensure the safe operation is shown in note 1 on page 5.

To avoid the EML3505 from exceeding the maximum junction temperature, the user should perform some thermal analysis during PCB design.

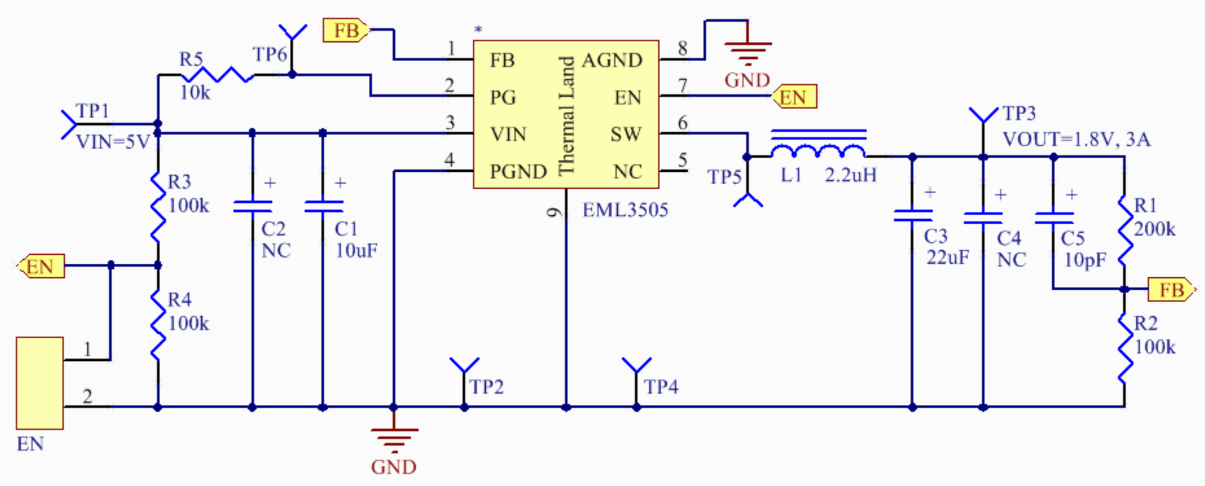
Guidelines for PCB Layout

To ensure proper operation of the EML3505, please note the following PCB layout guidelines:

1. The GND, SW and the VIN trace should be kept short, direct and wide.
2. VFB pin must be connected directly to the feedback resistors. Resistive divider R_1/R_2 must be connected parallel to the output capacitor C_{OUT}.
3. The Input capacitor C_{IN} must be connected to the pin VIN as close as possible.
4. Keep SW node away from the sensitive VFB node since this node has high frequency and voltage swing.
5. Keep the (–) plates of C_{IN} and C_{OUT} as close as possible.

Applications

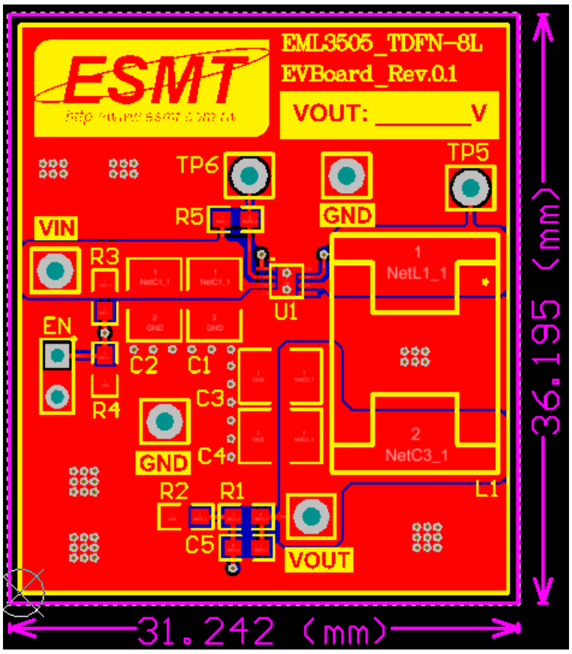
Typical schematic for PCB layout



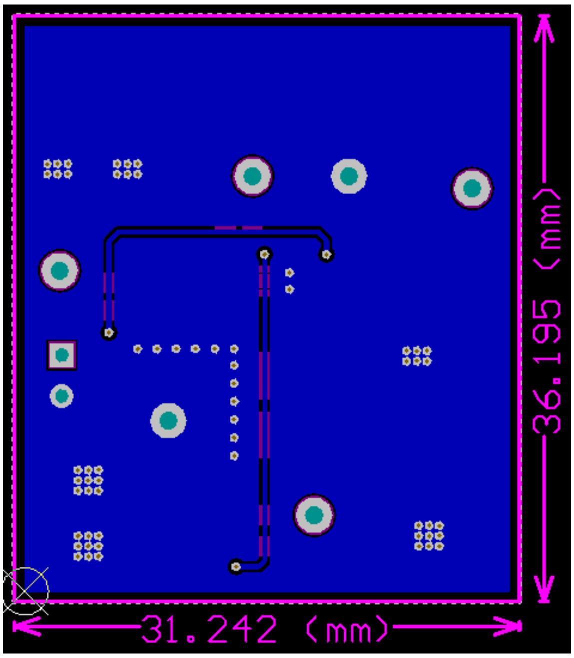
Note.

R3 and C4 are reserved locations for testing purposes. They are removed during normal applications.

Typical schematic for PCB layout (cont.)

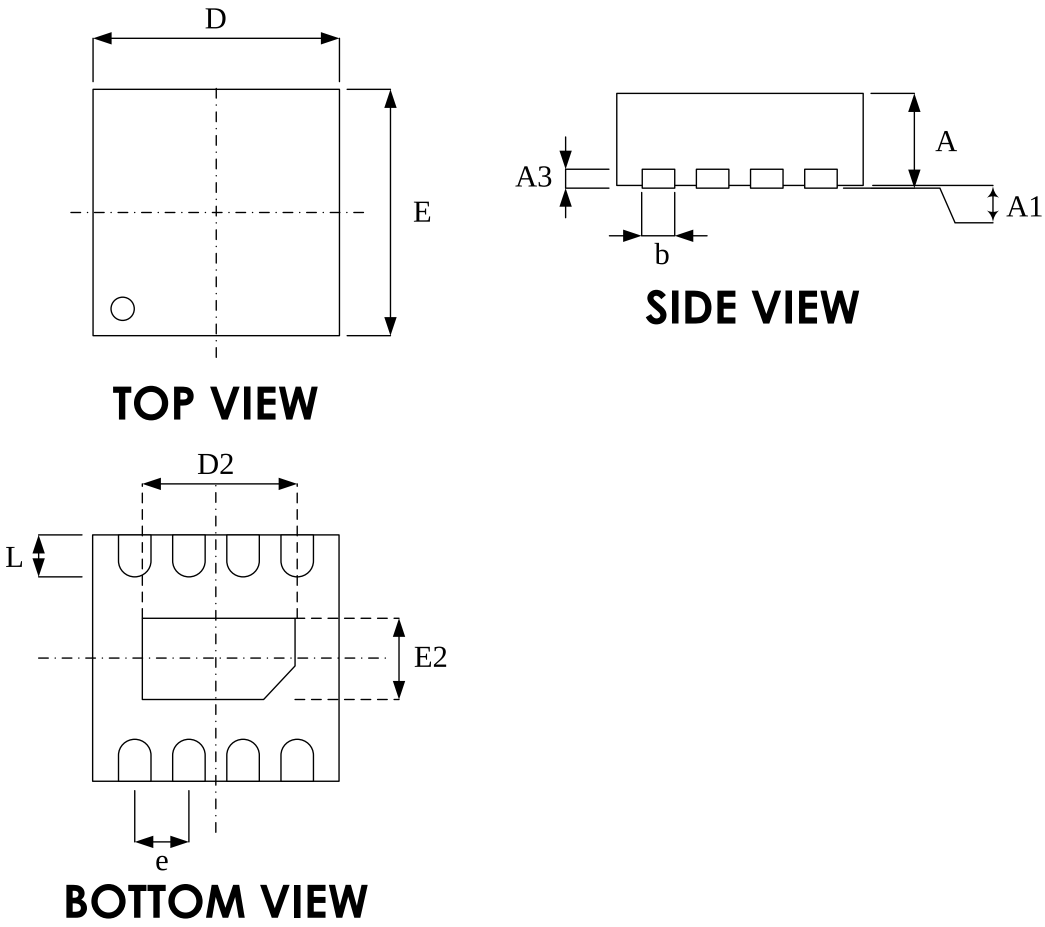


Top Layer



Bottom Layer

Package Outline Drawing
TDFN-8L (2x2 mm)



Symbol	Dimension in mm	
	Min	Max
A	0.70	0.80
A1	0.00	0.05
A3	0.18	0.25
b	0.18	0.30
D	1.90	2.10
E	1.90	2.10
e	0.50 BSC	
L	0.20	0.45

Exposed pad

	Dimension in mm	
	Min	Max
D2	1.10	1.30
E2	0.55	0.75

Revision History

Revision	Date	Description
0.1	2024.02.22	Initial version.
0.2	2024.04.24	1.Modified Order, Mark & Packing information 2.Modified Electrical Characteristics
0.3	2024.10.22	Modified Electrical Characteristics(Ron units)
1.0	2024.12.26	1.Remove preliminary and version to 1.0 2.Modified Feature(OVP) 3.Modified the picture name (Change PSM to PFM)

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