Features

- Wide Supply Voltage Range: 1.4V to 5.5V
- Low Quiescent Current
- Propagation Delay: 5.5μs (Max.)
- Rail to Rail input and output operation
- Internal Hysteresis: 20mV (Max.)
- Operating Temperature Range: -40˚C to +85˚C
- Available in Single and Dual versions
- Package types:
  - HT93111/HT93121: 5-pin SOT23, 8-pin SOP
  - HT93112/HT93122: 8-pin SOP

Applications

- Battery Level Detectors
- Alarm and Monitoring Circuits
- Logic Level Shifting or Translation
- Window Comparators
- Threshold Detectors
- RC Timers
- Multi-vibrators
- Mobile Communications and Notebooks
- RF/IR Receivers

General Description

The HT93111/HT93121/HT93112/HT93122 family of low power comparators offers the benefits of low power consumption, low offset voltage and low offset drift. The HT93111/HT93121 are offered in single channel and the HT93112/HT93122 are offered in dual channel. They have low propagation delay and have good PSRR and CMRR characteristics. These devices also provide full rail-to-rail input and output operation.

The devices operate with a single supply voltage as low as 1.4V and with a low supply current of 0.8μA/comparator (Typ.).

The HT93111/HT93112 family of comparators has push-pull output and supports rail-to-rail output swing and interfaces with TTL/CMOS logic. However, the HT93121/HT93122 family of comparators has open-drain output and can be used as a level-shifter for up to 6V using a pull-up resistor.

With their single wide range of supply voltage and low power consumption features coupled with their low offset voltage, these comparators are suitable for use in a wide range of applications. Besides, small-sized packages provide options for portable and space-restricted applications.

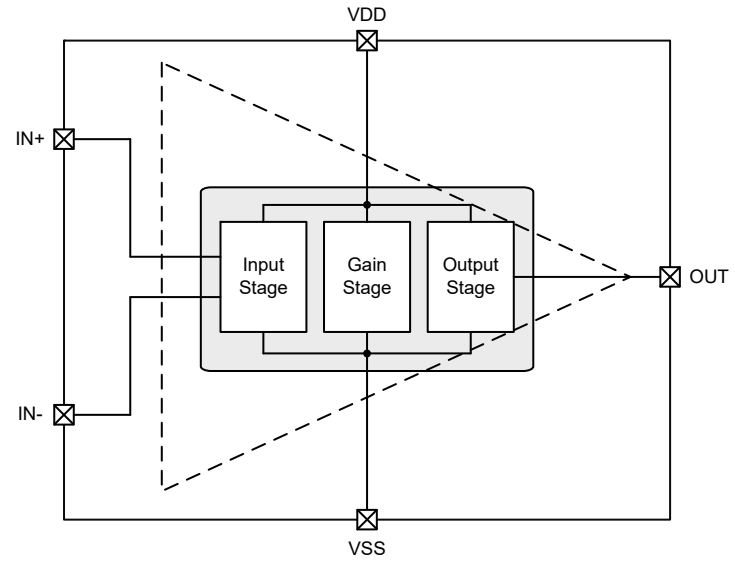
Selection Table

Part No.	Output Type	Operating Voltage	Channel Number	Latch Enable	Package	Marking
HT93111A	Push Pull	1.4V~5.5V	1	Y	SOT23-5	3111A
HT93111B					SOT23-5	3111B
HT93111C					SOT23-5	3111C
HT93111					8SOP	HT93111
HT93121A	Open Drain	1.4V~5.5V	1	Y	SOT23-5	3121A
HT93121B					SOT23-5	3121B
HT93121C					SOT23-5	3121C
HT93121					8SOP	HT93121
HT93112*	Push Pull	1.4V~5.5V	2	N	8SOP	HT93112
HT93122*	Open Drain	1.4V~5.5V	2	N	8SOP	HT93122

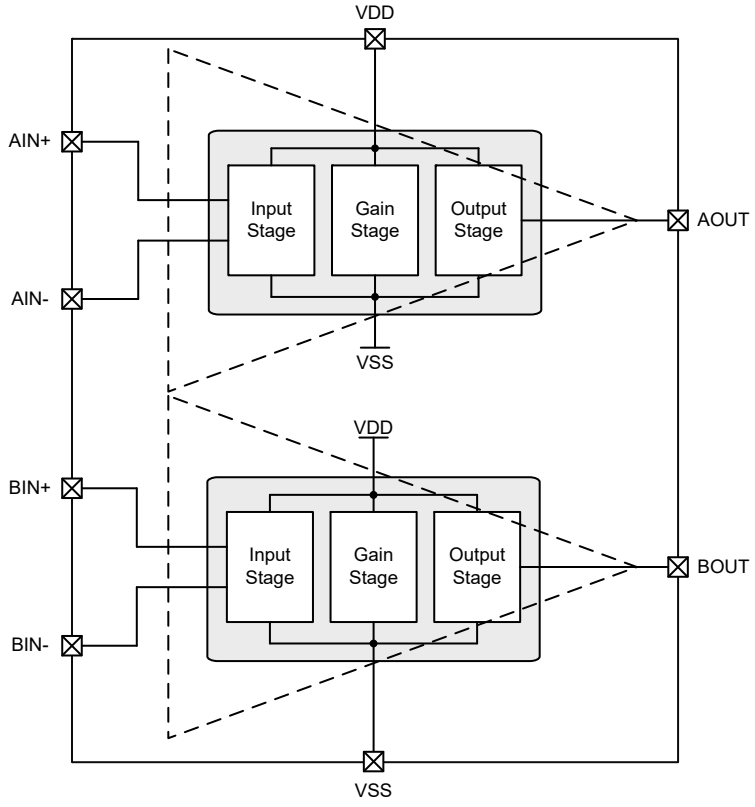
Note: * Under development

Block Diagram

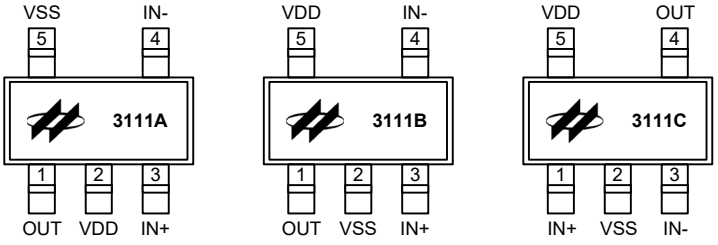
HT93111/HT93121



HT93112/HT93122



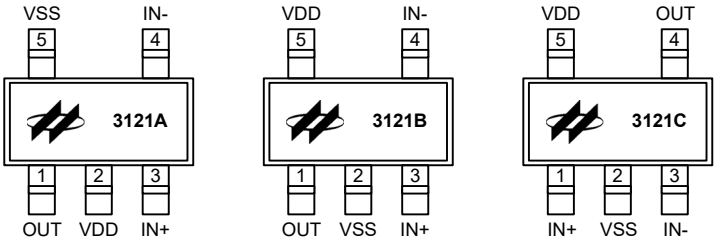
Pin Assignment



HT93111A
SOT23-5-A

HT93111B
SOT23-5-B

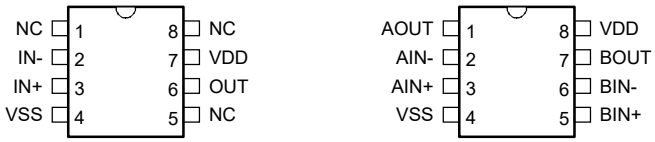
HT93111C
SOT23-5-C



HT93121A
SOT23-5-A

HT93121B
SOT23-5-B

HT93121C
SOT23-5-C



HT93111/HT93121
8 SOP-A

HT93112/HT93122
8 SOP-A

Pin Description

HT93111/HT93121

Pin Name	Type	Description
OUT	AO	Push-Pull Output for HT93111; Open-Drain Output for HT93121
IN+	AI	Non-inverting Input
IN-	AI	Inverting Input
VDD	PWR	Positive Power Supply
VSS	PWR	Negative Power Supply

Legend: AI: Analog Input; AO: Analog Output; I: Input; PWR: Power.

HT93112/HT93122

Pin Name	Type	Description
AOUT	AO	Push-Pull Output for HT93112 CMP-A; Open-Drain Output for HT93122 CMP-A
AIN+	AI	Non-inverting Input for CMP-A
AIN-	AI	Inverting Input for CMP-A
BOUT	AO	Push-Pull Output for HT93112 CMP-B; Open-Drain Output for HT93122 CMP-B
BIN+	AI	Non-inverting Input for CMP-B
BIN-	AI	Inverting Input for CMP-B
VDD	PWR	Positive Power Supply
VSS	PWR	Negative Power Supply

Legend: AI: Analog Input; AO: Analog Output; PWR: Power.

Absolute Maximum Ratings

Supply Voltage ..... V_{SS}-0.3V to 6.0V

Input Voltage ..... V_{SS}-0.3V to V_{DD}+0.3V

Storage Temperature ..... -60°C to 150°C

Operating Temperature ..... -40°C to 85°C

I_{OH} Total ..... -80mA

I_{OL} Total 80mA

Total Power Dissipation 500mW

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to these devices. Functional operation of these devices at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Electrical Characteristics

HT93111/HT93112

Unless otherwise indicated, V_{DD}=1.4V~5.5V, V_{SS}=GND, Ta=25°C, V_{IN+}=V_{DD}/2, V_{IN-}=V_{SS}, V_L=V_{DD}/2, R_L=1MΩ to V_L.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Input Characteristics						
V_{OS}	Input Offset Voltage	V_{CM}=V_{SS}	-12	—	12	mV
$\Delta V_{OS}/\Delta T_A$	Input Offset Voltage Drift with Temperature	V_{CM}=V_{SS}, Ta=-40°C~85°C	—	±2	—	μV/°C
I_B	Input Bias Current	V_{CM}=V_{SS}	—	38	—	pA
I_{OS}	Input Offset Current	V_{CM}=V_{SS}	—	1	—	pA
V_{CMR}	Common Mode Input Voltage Range	—	V_{SS}-0.3	—	V_{DD}+0.3	V
V_{HYST}	Input Hysteresis Voltage	V_{CM}=V_{SS} (1)	-20	—	20	mV
V_{IH}	Latch Enable Pin High Input Voltage	HT93111 only	V_{SS}	—	0.2V_{DD}	V
V_{IL}	Latch Enable Pin Low Input Voltage	HT93111 only	0.8V_{DD}	—	V_{DD}	V
CMRR	Common Mode Rejection	V_{DD}=5V, V_{CM}=-0.3V to 5.3V	67	85	—	dB
		V_{DD}=5V, V_{CM}=2.5V to 5.3V	65	80	—	
		V_{DD}=5V, V_{CM}=-0.3V to 2.5V	65	85	—	
PSRR	Power Supply Rejection	V_{CM}=V_{SS}	75	90	—	dB
A_{OL}	DC Open-Loop Gain (Large Signal)	R_L=50kΩ to V_L, V_{OUT}=0.1V to V_{DD}-0.1V	—	105	—	dB

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Output Characteristics						
t_{PHL}	Propagation Delay (High-to-Low)	V_{DD}=1.4V to 1.6V, V_{IN+}=V_{DD}/2, Overdrive=100mV, C_L=30pF, Ta=-40°C~85°C	—	1.4	1.6	μs
		V_{DD}=1.6V to 5.5V, V_{IN+}=V_{DD}/2, Overdrive=100mV, C_L=30pF, Ta=-40°C~85°C	—	1.4	1.6	
t_{PLH}	Propagation Delay (Low-to-High)	V_{DD}=1.4V to 1.6V, V_{IN+}=V_{DD}/2, Overdrive=100mV, C_L=30pF, Ta=-40°C~85°C	—	2.3	2.4	μs
		V_{DD}=1.6V to 5.5V, V_{IN+}=V_{DD}/2, Overdrive=100mV, C_L=30pF, Ta=-40°C~85°C	—	4.2	5.5	
t_{PDS}	Propagation Delay Skew	V_{DD}=1.4V to 5.5V, V_{IN+}=V_{DD}/2, Overdrive=100mV, C_L=30pF (2)	—	±1	—	μs
t_R	Rise Time	V_{IN+}=V_{DD}/2, Overdrive=100mV, C_L=30pF	—	5	—	ns
t_F	Fall Time	V_{IN+}=V_{DD}/2, Overdrive=100mV, C_L=30pF	—	5	—	ns
t_{LPD}	Latch Propagation Delay	HT93111 only	—	20	—	ns
V_{OL}	Minimum Output Voltage Swing	R_L=50kΩ to V_L, 0.5V input overdrive	—	—	V_{SS}+10	mV
V_{OH}	Maximum Output Voltage Swing	R_L=50kΩ to V_L, 0.5V input overdrive	V_{DD}-10	—	—	
I_{SC}	Output Short Circuit Current	V_{DD}=1.4V	—	±2	—	mA
		V_{DD}=5.5V	—	±30	—	mA
Power Supply						
V_{DD}	Supply Voltage	—	1.4	—	5.5	V
I_Q	Quiescent Current per Comparator	OUT=High, Ta=25°C	—	0.8	1.3	μA
		OUT=Low, Ta=25°C	—	1.3	2.0	μA
Temperature						
Ta	Operating Temperature Range	—	-40	—	85	°C

Note: 1. The input offset voltage is the average of the input-referred trip points. The input hysteresis is the difference between the input-referred trip points.

2. Propagation Delay Skew is defined as: t_{PDS}=t_{PLH}-t_{PHL}.

HT93121/HT93122

Unless otherwise indicated, V_{DD}=1.4V~5.5V, V_{SS}=GND, Ta=25°C, V_{IN+}=V_{DD}/2, V_{IN-}=V_{SS}, R_{PU}=2.74kΩ to V_{PU}=V_{DD}.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Input Characteristics						
V_{OS}	Input Offset Voltage	V_{CM}=V_{SS}	-12	—	12	mV
$\Delta V_{OS}/\Delta T_A$	Input Offset Voltage Drift with Temperature	V_{CM}=V_{SS}, Ta=-40°C~85°C	—	±2	—	μV/°C
I_B	Input Bias Current	V_{CM}=V_{SS}	—	38	—	pA
I_{OS}	Input Offset Current	V_{CM}=V_{SS}	—	1	—	pA
V_{CMR}	Common Mode Input Voltage Range	—	V_{SS}-0.3	—	V_{DD}+0.3	V
V_{HYST}	Input Hysteresis Voltage	V_{CM}=V_{SS} (1)	-20	—	20	mV
V_{IH}	Latch Enable Pin High Input Voltage	HT93121 only	V_{SS}	—	0.2V_{DD}	V
V_{IL}	Latch Enable Pin Low Input Voltage	HT93121 only	0.8V_{DD}	—	V_{DD}	V

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CMRR	Common Mode Rejection	V_{DD}=5V, V_{CM}=-0.3V to 5.3V	67	85	—	dB
		V_{DD}=5V, V_{CM}=2.5V to 5.3V	65	80	—	
		V_{DD}=5V, V_{CM}=-0.3V to 2.5V	65	85	—	
PSRR	Power Supply Rejection	V_{CM}=V_{SS}	75	90	—	dB
A_{OL}	DC Open-Loop Gain (Large Signal)	R_{PU}=2.74kΩ to V_{PU}, V_{OUT}=0.1V to V_{DD}-0.1V	—	105	—	dB
Output Characteristics						
t_{PHL}	Propagation Delay (High-to-Low)	V_{DD}=1.4V to 1.6V, V_{IN+}=V_{DD}/2, Overdrive=100mV, C_L=30pF, Ta=-40°C~85°C	—	1.4	1.6	μs
		V_{DD}=1.6V to 5.5V, V_{IN+}=V_{DD}/2, Overdrive=100mV, C_L=30pF, Ta=-40°C~85°C	—	1.4	1.6	
t_{PLH}	Propagation Delay (Low-to-High)	V_{DD}=1.4V to 1.6V, V_{IN+}=V_{DD}/2, Overdrive=100mV, C_L=30pF, Ta=-40°C~85°C	—	2.3	2.4	μs
		V_{DD}=1.6V to 5.5V, V_{IN+}=V_{DD}/2, Overdrive=100mV, C_L=30pF, Ta=-40°C~85°C	—	4.2	5.5	
t_{PDS}	Propagation Delay Skew	V_{DD}=1.4V to 5.5V, V_{IN+}=V_{DD}/2, Overdrive=100mV, C_L=30pF (2)	—	±1	—	μs
t_F	Fall Time	V_{IN+}=V_{DD}/2, Overdrive=100mV, C_L=30pF	—	5	—	ns
t_{LPD}	Latch Propagation Delay	HT93121 only	—	20	—	ns
V_{OL}	Minimum Output Voltage Swing	R_{PU}=2.74kΩ to V_{PU}, 0.5V input overdrive	—	—	V_{SS}+10	mV
I_{SC}	Output Short Circuit Current	V_{DD}=1.4V	—	2	—	mA
		V_{DD}=5.5V	—	30	—	mA
Power Supply						
V_{DD}	Supply Voltage	—	1.4	—	5.5	V
I_Q	Quiescent Current per Comparator	OUT=High, Ta=25°C	—	0.8	1.3	μA
		OUT=Low, Ta=25°C	—	1.3	2.0	μA
Temperature						
Ta	Operating Temperature Range	—	-40	—	85	°C

Note: 1. The input offset voltage is the average of the input-referred trip points. The input hysteresis is the difference between the input-referred trip points.

2. Propagation Delay Skew is defined as: t_{PDS}=t_{PLH}-t_{PHL}.

Special Function Description

Internal Hysteresis

The HT93111/HT93121/HT93112/HT93122 family has an internally-set hysteresis which has two trip points, one for the rising input voltage and the other for the falling input voltage. The internally-set hysteresis is large enough to eliminate output glitch caused by the comparator's own input noise voltage. The Figure 2 and Figure 3 show this behavior.

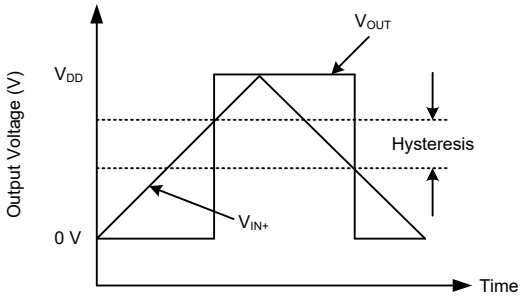


Figure 2. Internal Hysteresis with Non-Inverting Output

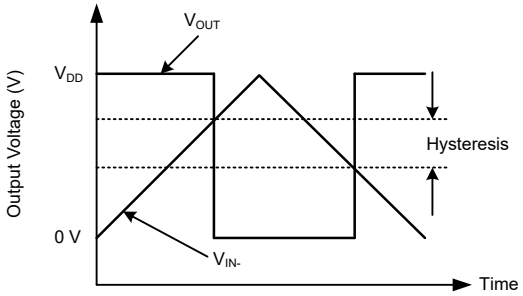


Figure 3. Internal Hysteresis with Inverting Output

External Hysteresis

More flexible hysteresis is achieved by using external resistors. Hysteresis reduces output chattering when one input is slowly going past the other input and thus reduces dynamic supply current. It also helps in systems where it is best not to switch between states too frequently, e.g., air conditioner thermostatic control.

Non-Inverting Circuit with External Hysteresis

Figure 4 shows a non-inverting circuit with external hysteresis using just two resistors. The resulting external hysteresis diagram for the non-inverting circuit is shown in Figure 5. The trip points for the non-inverting circuit with external hysteresis are:

$$V_{TH} = \frac{R_1+R_2}{R_2} V_{REF} - \frac{R_1}{R_2} V_{OL}$$

$$V_{TL} = \frac{R_1+R_2}{R_2} V_{REF} - \frac{R_1}{R_2} V_{OH}$$

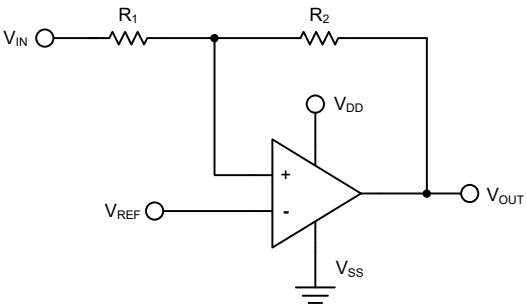


Figure 4. Non-Inverting Circuit with External Hysteresis

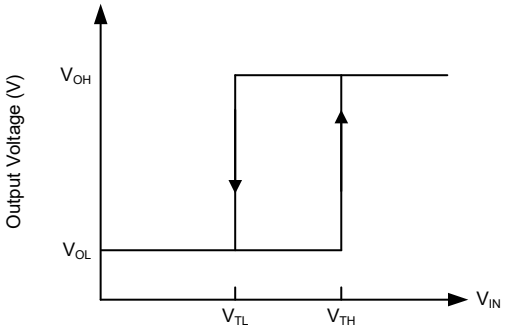


Figure 5. External Hysteresis Diagram for Non-Inverting Circuit

Inverting Circuit with External Hysteresis

Figure 6 shows an inverting circuit with external hysteresis using just three resistors. In order to simplify the circuit, the Thevenin equivalent circuit of Figure 6 is shown in Figure 7. The resulting external hysteresis diagram for the inverting circuit is shown in Figure 8. The trip points for the inverting circuit with external hysteresis are:

$$V_{TH} = \frac{R_T}{R_T+R_3} V_{OH} + \frac{R_3}{R_T+R_3} V_T$$

$$V_{TL} = \frac{R_T}{R_T+R_3} V_{OL} + \frac{R_3}{R_T+R_3} V_T$$

Where

$$R_T = \frac{R_1 R_2}{R_1+R_2}$$

$$V_T = \frac{R_2}{R_1+R_2} V_{DD}$$

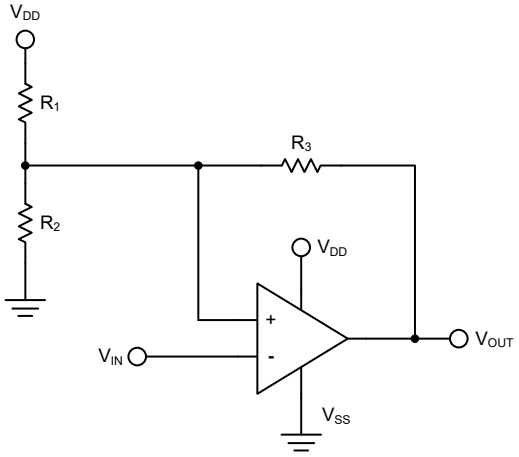


Figure 6. Inverting Circuit with External Hysteresis

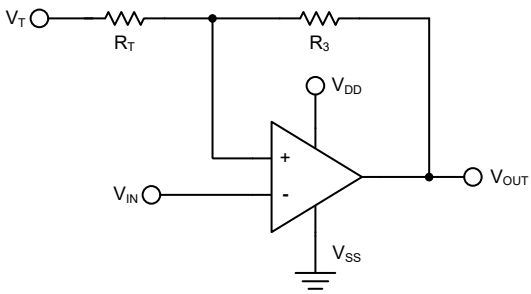


Figure 7. Thevenin Equivalent Circuit

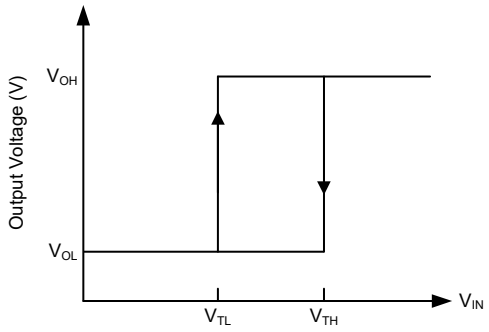
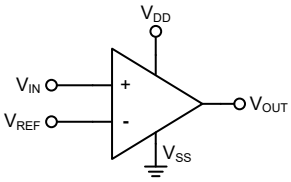


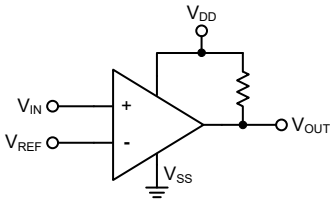
Figure 8. External Hysteresis Diagram for Inverting Circuit

Application Circuits

HT93111/HT93121

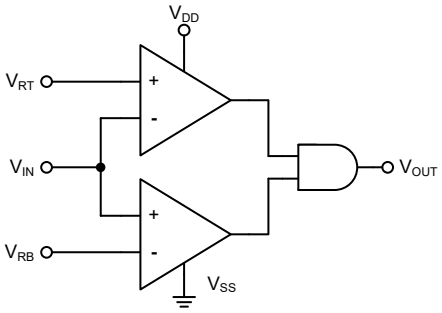


HT93111

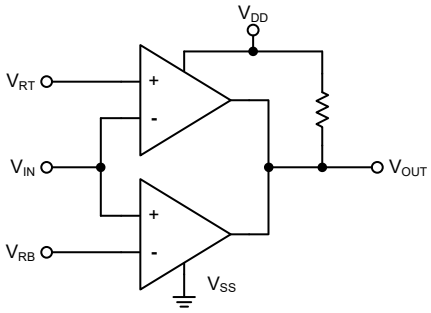


HT93121

HT93112/HT93122



HT93112 Window Comparator



HT93122 Window Comparator

Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

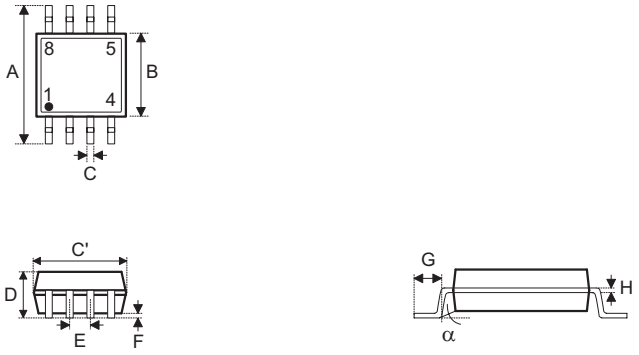
Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

• Further Package Information (include Outline Dimensions, Product Tape and Reel Specifications)

• Packing Meterials Information

• Carton information

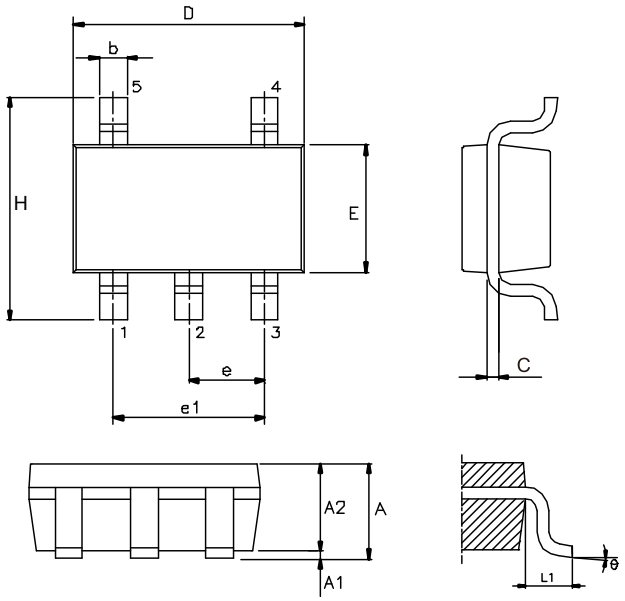
8-pin SOP (150mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A		0.236 BSC	
B		0.154 BSC	
C	0.012	—	0.020
C′		0.193 BSC	
D	—	—	0.069
E		0.050 BSC	
F	0.004	—	0.010
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A		6.00 BSC	
B		3.90 BSC	
C	0.31	—	0.51
C′		4.90 BSC	
D	—	—	1.75
E		1.27 BSC	
F	0.10	—	0.25
G	0.40	—	1.27
H	0.10	—	0.25
α	0°	—	8°

5-pin SOT23 Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	—	0.057
A1	—	—	0.006
A2	0.035	0.045	0.051
b	0.012	—	0.020
C	0.003	—	0.009
D		0.114 BSC	
E		0.063 BSC	
e		0.037 BSC	
e1		0.075 BSC	
H		0.110 BSC	
L1		0.024 BSC	
θ	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	—	1.45
A1	—	—	0.15
A2	0.90	1.15	1.30
b	0.30	—	0.50
C	0.08	—	0.22
D		2.90 BSC	
E		1.60 BSC	
e		0.95 BSC	
e1		1.90 BSC	
H		2.80 BSC	
L1		0.60 BSC	
θ	0°	—	8°