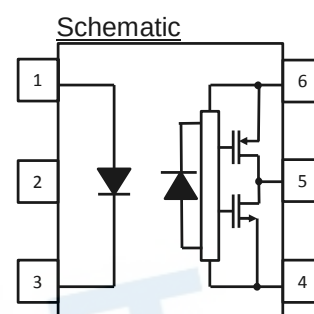
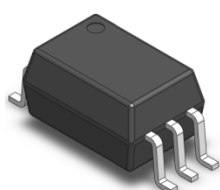


6 PIN SDIP IGBT/MOSFET 2.5A Output Current GATE DRIVER PHOTOCOUPLER ELS3120-G Series



Features:

- Compliance Halogens Free
(Br < 900 ppm, Cl < 900 ppm, Br+Cl < 1500 ppm)
- Rail-to-rail output voltage
- Guaranteed performance from -40 to 110°C
- Peak Output Current : $I_{OP} = 2.5A$ (max)
- Threshold Input Current: $I_{FLH} = 5$ mA (max)
- High isolation voltage between input and output (Viso=5000 V rms)
- Pb free and RoHS compliant.
- UL and cUL approved
- VDE approved
- SEMKO approved
- NEMKO approved
- DEMKO approved
- FIMKO approved
- CQC approved

Pin Configuration

- 1, Anode
- 2, No Connection
- 3, Cathode
- 4, V_{EE}
- 5, V_{OUT}
- 6, V_{CC}

Note A : 0.1 μ F bypass capacitor must be connected between pins 4 and 6

Description

The ELS3120 consists of an infrared light emitting diodes coupled to an integrated circuit with a power output stage.

The photo coupler has an internal shield that provides guaranteed common-mode transient immunity of ± 25 kV/ μ s. It is suitable for direct gate driving circuit for IGBTs or power MOSFETs.

Applications

- Isolated IGBT/Power MOSFET Gate Drive
- Uninterruptible power supply
- Inverters
- Home appliances, such as fan heaters, etc.

Absolute Maximum Ratings (Ta=25°C)

	Parameter	Symbol	Rating	Unit
Input	Forward current	I _F	25	mA
	Pulse Forward Current* ¹	I _{FP}	1	A
	Reverse voltage	V _R	5	V
Output	"H" Peak Output current	I _{OPH}	2.5	A
	"L" Peak Output Current	I _{OPL}	2.5	A
	Peak Output Voltage	V _O	30	V
	Supply Voltage	V _{CC} - V _{EE}	15 to 30	V
	Operating frequency	f	50	kHz
	Isolation voltage * ²	V _{ISO}	5000	V rms
	Total Power Dissipation	P _T	300	mW
	Operating temperature	T _{OPR}	-40 ~ +110	°C
	Storage temperature	T _{STG}	-55 ~ +125	°C
	Soldering temperature * ³	T _{SOL}	260	°C

Notes:

*1 Pulse width ≤ 1μs, 300pps.

*2 AC for 1 minute, R.H.= 40 ~ 60% R.H. In this test, pins 1 to 3 are shorted together, and pins 4 to 6 are shorted together.

*3 For 10 seconds.

Electro-Optical Characteristics

Input

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Forward Voltage	V_F	-	-	1.8	V	$I_F = 10\text{mA}$
Reverse Current	V_R	5	-	-	V	$I_R = 10\mu\text{A}$

Output

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
High level supply current	I_{CCH}	-	1.4	3.2	mA	$I_F=10\text{mA}$, $V_{CC}=30\text{V}$ $V_O = \text{Open}$
Low level supply current	I_{CCL}	-	1.5	3.2		$I_F=0\text{mA}$, $V_{CC}=30\text{V}$ $V_O = \text{Open}$

Transfer Characteristics

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
High Level Output Current*4	I_{OH}	-	-2.5	-1	A	$I_F=10\text{mA}$, $V_{CC}=30\text{V}$, $V_O=V_{CC}-3\text{V}$
		-	-	-2.5		$I_F=10\text{mA}$, $V_{CC}=30\text{V}$, $V_O=V_{CC}-6\text{V}$
Low Level Output Current*4	I_{OL}	1	2.5	-		$I_F=0\text{mA}$, $V_{CC}=30\text{V}$, $V_O=V_{EE}+3\text{V}$
		2.5	-	-		$I_F=0\text{mA}$, $V_{CC}=30\text{V}$, $V_O=V_{EE}+6\text{V}$
High Level Output Voltage	V_{OH}	$V_{CC}-0.3$	29.8	-	V	$I_F=10\text{mA}$, $V_{CC}=30\text{V}$, $I_O=-100\text{mA}$
Low Level Output Voltage	V_{OL}		0.1	$V_{EE}+0.25$	V	$I_F=0\text{mA}$, $V_{CC}=30\text{V}$, $I_O=100\text{mA}$
Input Threshold Current	I_{FLH}	-	-	5	mA	$V_{CC}=15$ or 30V , $V_O > 5\text{V}$
Input Threshold Voltage	V_{FHL}	0.8	-	-	V	$V_{CC}=15$ or 30V , $V_O < 5\text{V}$
Under Voltage Lockout Threshold	V_{UVLO+}	11.0	-	13.5	V	$I_F=10\text{mA}$, $V_O > 5\text{V}$
Under Voltage Lockout Threshold	V_{UVLO-}	9.5	-	12.5	V	$I_F=10\text{mA}$, $V_O < 5\text{V}$

Switching Characteristics

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
Propagation delay time to output High level	t_{PLH}	50	150	300	ns	$I_F = 7 \text{ to } 16\text{mA}$ $V_{CC} = 15 \text{ to } 30\text{V}$ $C_g = 10\text{nF}$, $R_g = 10\Omega$, $f = 10\text{kHz}$, $T_A = 25^\circ\text{C}$ Duty Cycle=50%,
Propagation delay time to output Low level	t_{PHL}	50	150	300	ns	
Pulse width distortion	$ t_{PHL} - t_{PLH} $	-	-	100	ns	
Propagation Delay Skew*5	t_{PSK}	-	-	150	ns	
Output rise time	t_r	-	80	-	ns	
Output fall time	t_f	-	80	-	ns	
Common Mode Transient Immunity at Logic High*6	CM_H	25	-	-	kV/ μS	$I_F = 10\text{mA}$, $V_{CC} = 30\text{V}$, $T_A = 25^\circ\text{C}$ $V_{CM} = 1500\text{V}$
Common Mode Transient Immunity at Logic Low*7	CM_L	25	-	-	kV/ μS	$I_F = 0\text{mA}$, $V_{CC} = 30\text{V}$, $T_A = 25^\circ\text{C}$ $V_{CM} = 1500\text{V}$

Notes:

*4 Max. pulse width=10 μs , max. duty cycle =1%

*5 Propagation delay skew is defined as the difference between the largest and smallest propagation delay times (i.e. t_{PHL} or t_{PLH}) of multiple samples. Evaluations of these samples are conducted under identical test conditions (supply voltage, input current, temperature, etc).

*6 Common mode transient immunity at output high is the maximum tolerable negative dv/dt on the trailing edge of the common mode impulse signal, V_{CM} , to assure that the output will remain high (i.e. $V_O > 15.0\text{V}$)

*7 Common mode transient immunity at output low is the maximum tolerable positive dv/dt on the leading edge of the common mode pulse signal, V_{CM} , to assure that the output will remain low (i.e. $V_O < 1.0\text{V}$)

Typical Electro-Optical Characteristics Curves

Fig.1 Forward Voltage vs. Ambient Temperature

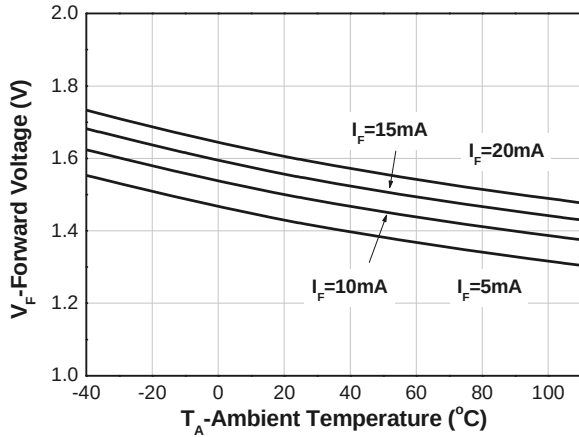


Fig.2 Output High Voltage vs. Output High Current

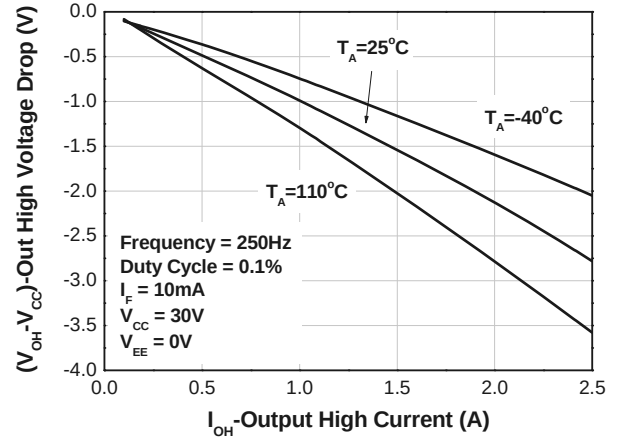


Fig. 3 Output High Voltage Drop vs. Ambient Temperature

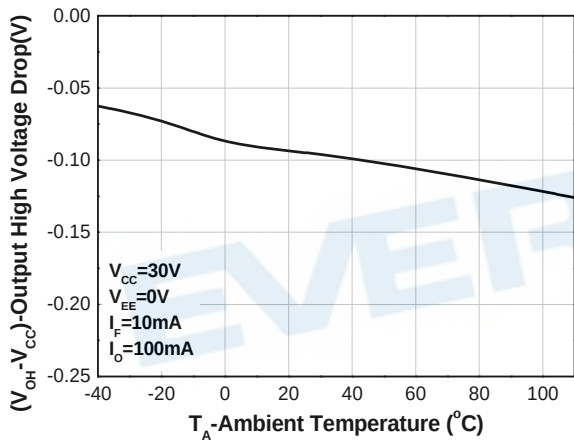


Fig.4 Output Low Voltage vs. Output Low Current

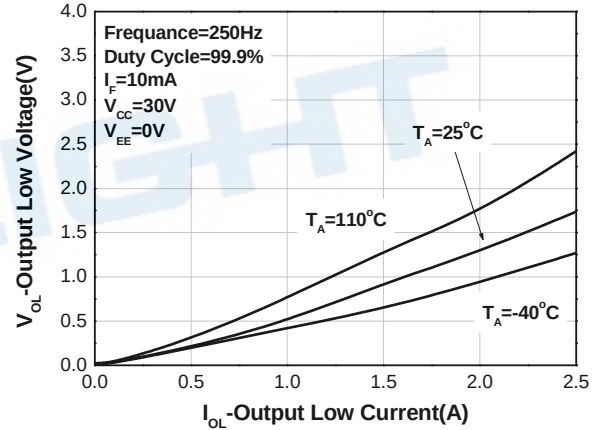


Fig. 5 Output Low Voltage vs. Ambient Temperature

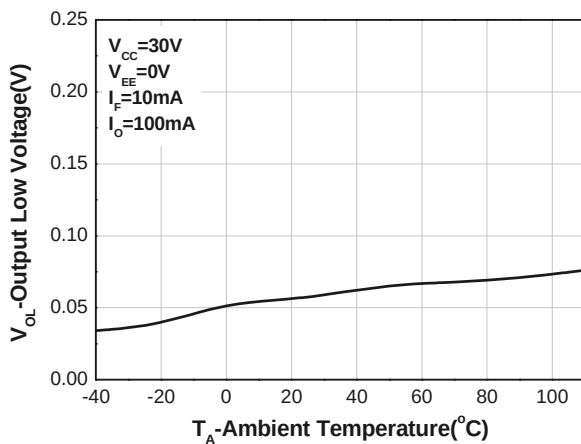


Fig.6 Supply Current vs. Ambient Temperature

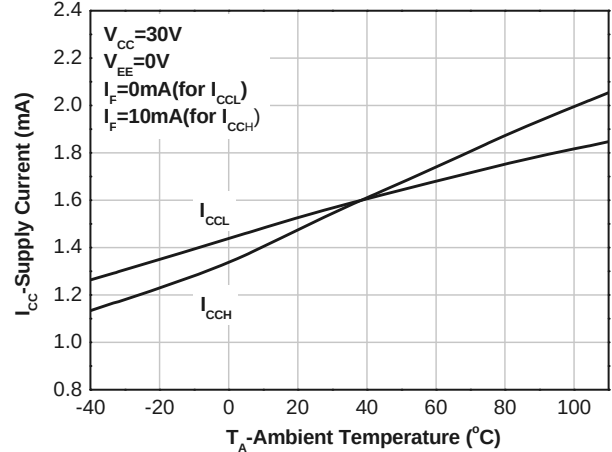


Fig.7 Supply Current vs Supply voltage

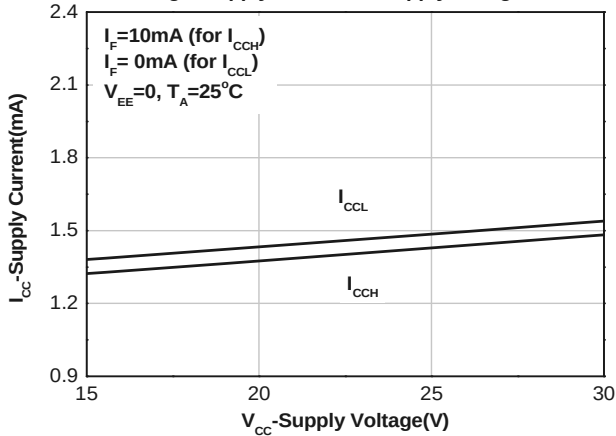


Fig.8 Threshold Input Current vs. Ambient Temperature

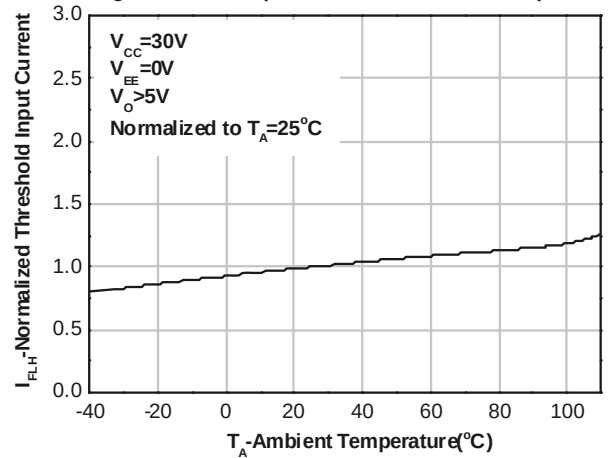


Fig 9. Under Voltage Lockout

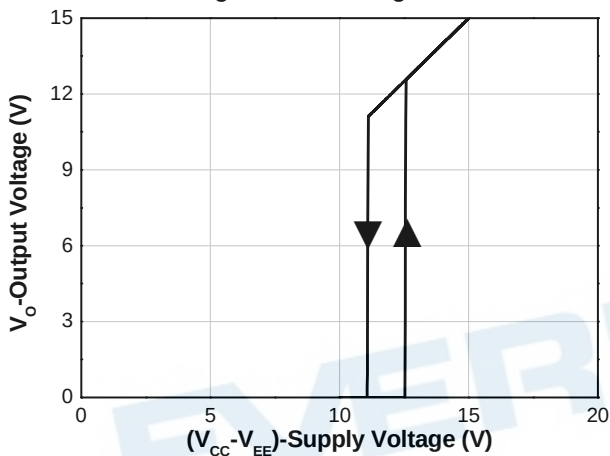


Fig.10 Propagation Delay vs Supply Voltage

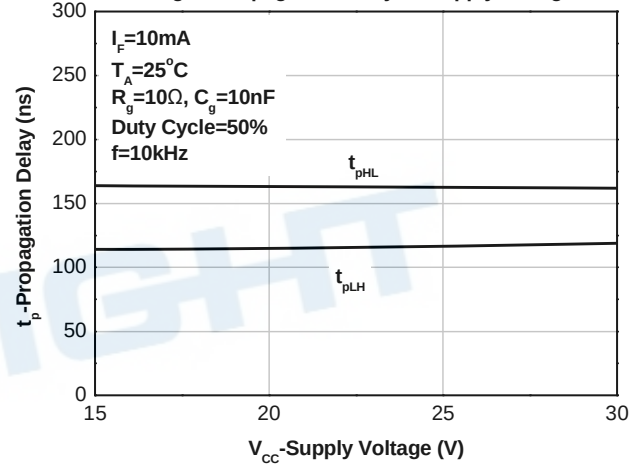


Fig.11 Propagation Delay vs LED Forward Current

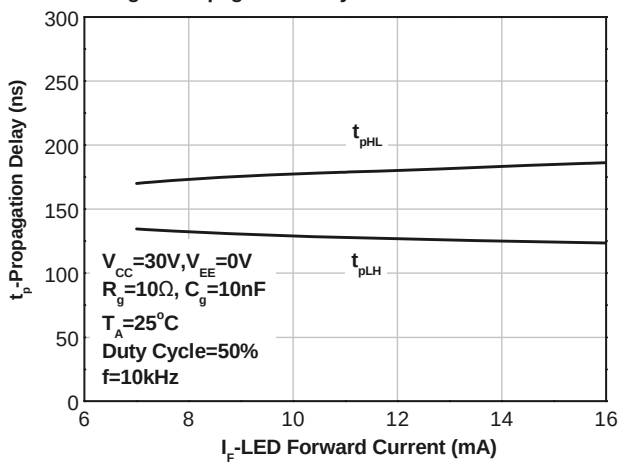


Fig.12 Propagation Delay vs. Ambient Temperature

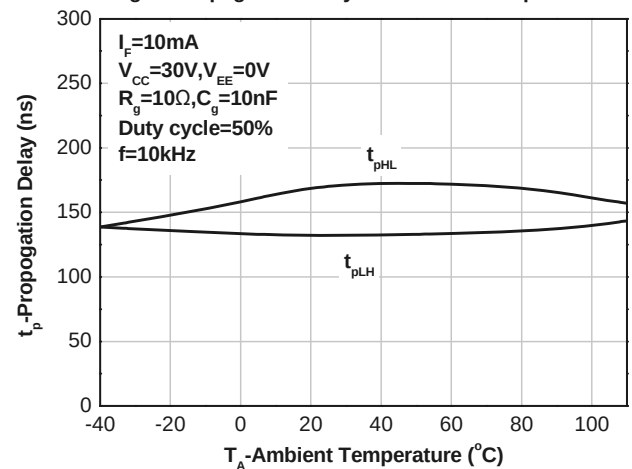


Fig.13 Propagation Delay vs. Serise Load Resistance

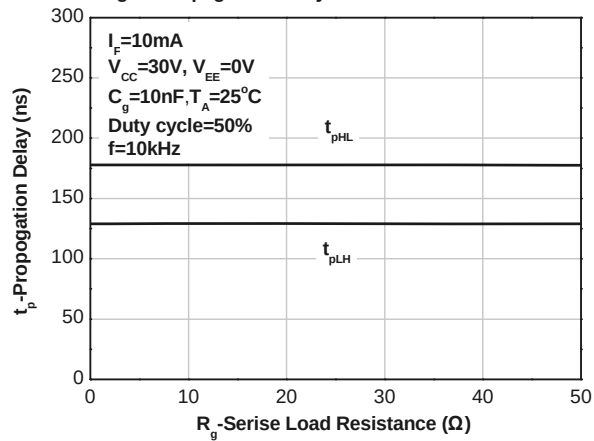


Fig.14 Propagation Delay vs. Load Capacitance

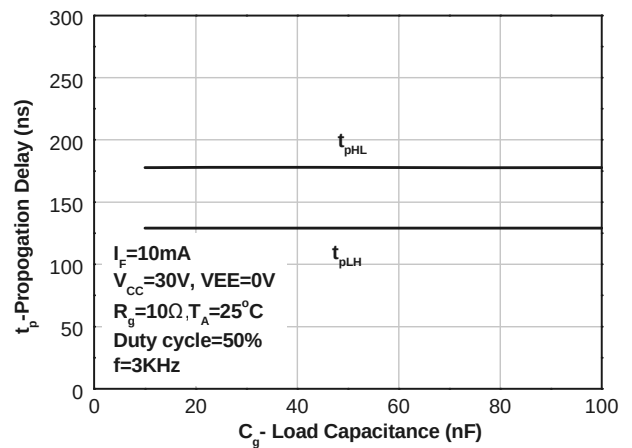


Fig. 15 I_{OH} Test circuit

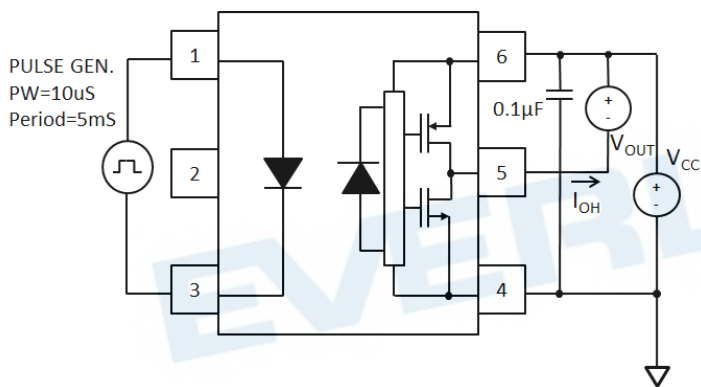


Fig. 16 I_{OL} Test circuit

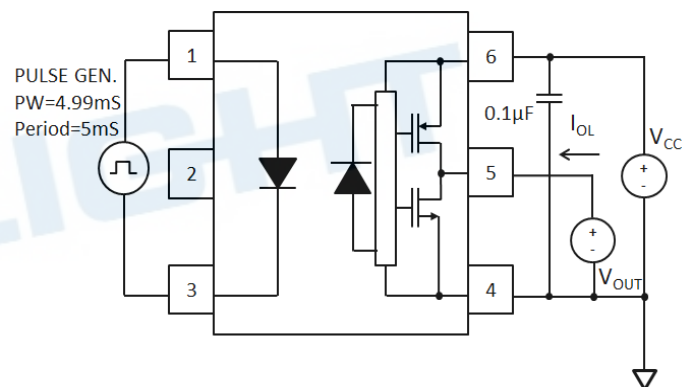


Fig. 17 V_{OH} Test circuit

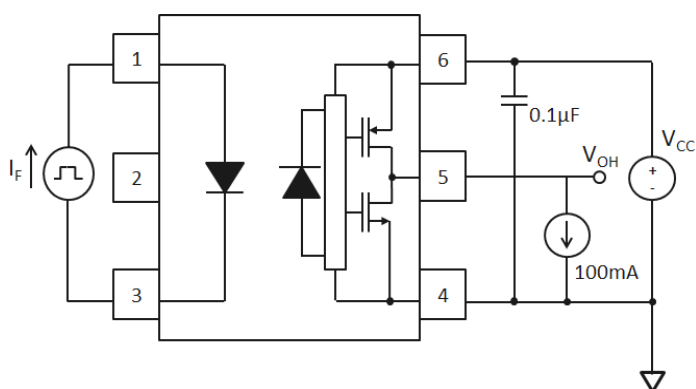


Fig. 18 V_{OL} Test circuit

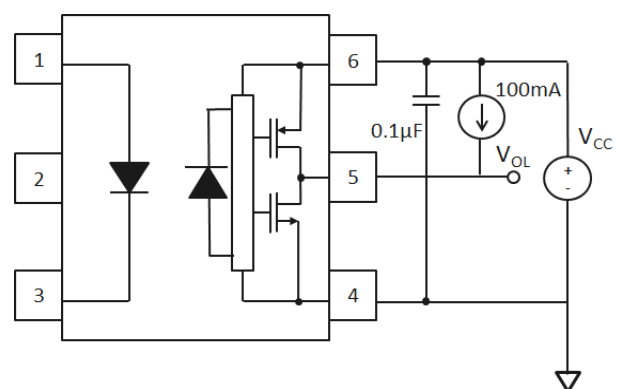


Fig. 19 I_{FHL} Test circuit

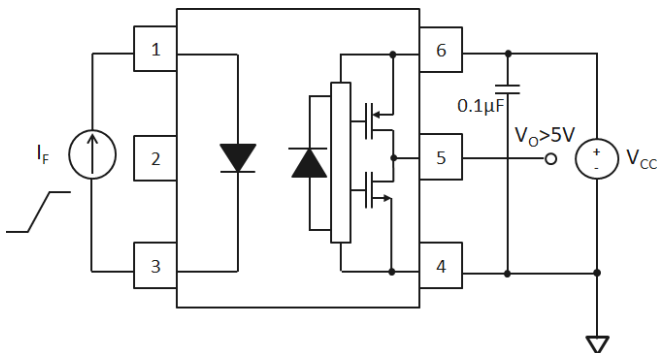


Fig. 20 UVLO Test circuit

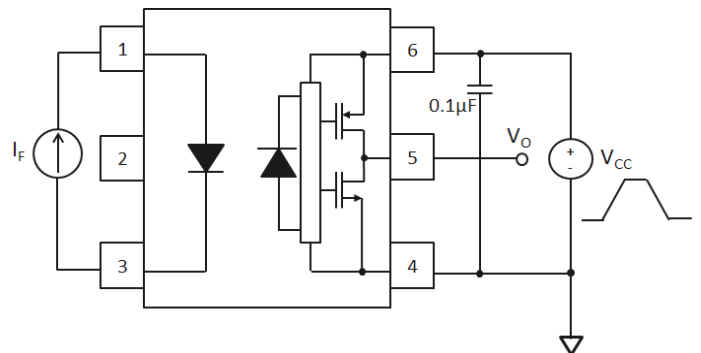


Fig. 21 Switching Time Test circuit

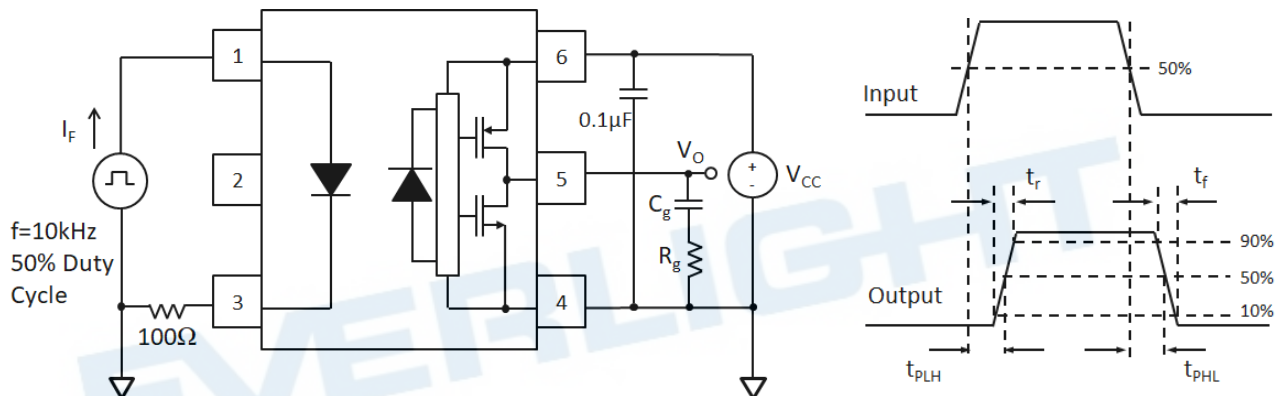
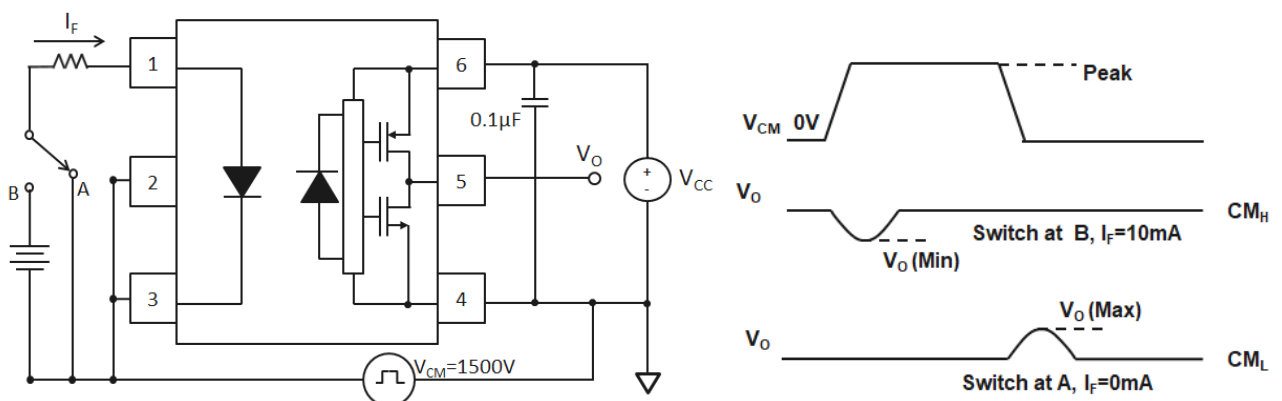


Fig. 22 CMR Test circuit



Order Information

Part Number

ELS3120X(Y)-VG

Note

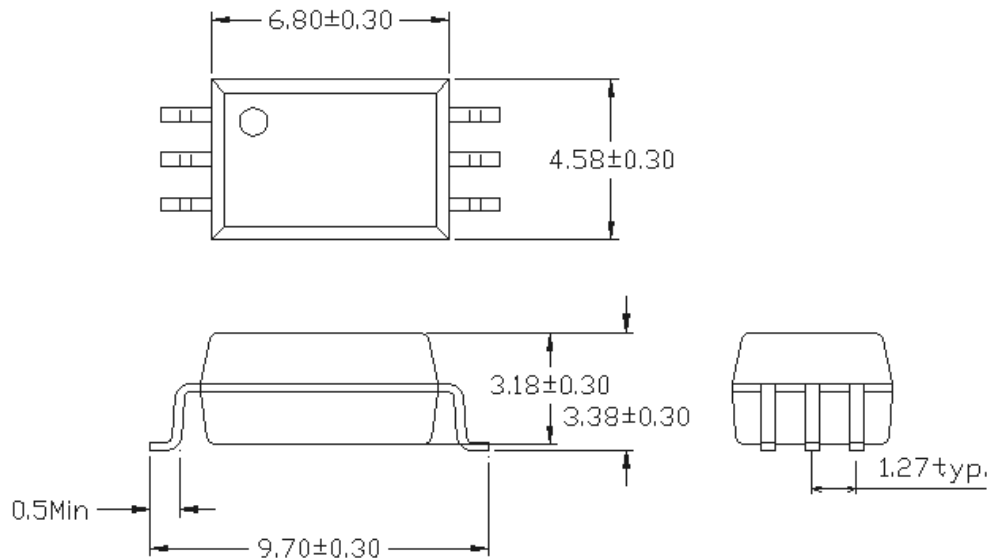
EL = denotes EVERLIGHT
S3120 = part no.
X = lead type(P,W)
Y = Tape and reel option (TA, TB)
V = VDE (optional)
G = Halogens free

Option	Description	Packing quantity
P(TA)	Surface mount lead form + TA tape & reel option	1000 units per reel
P(TB)	Surface mount lead form + TB tape & reel option	1000 units per reel
W(TA)	Surface mount lead form + TA tape & reel option	1000 units per reel
W(TB)	Surface mount lead form + TB tape & reel option	1000 units per reel

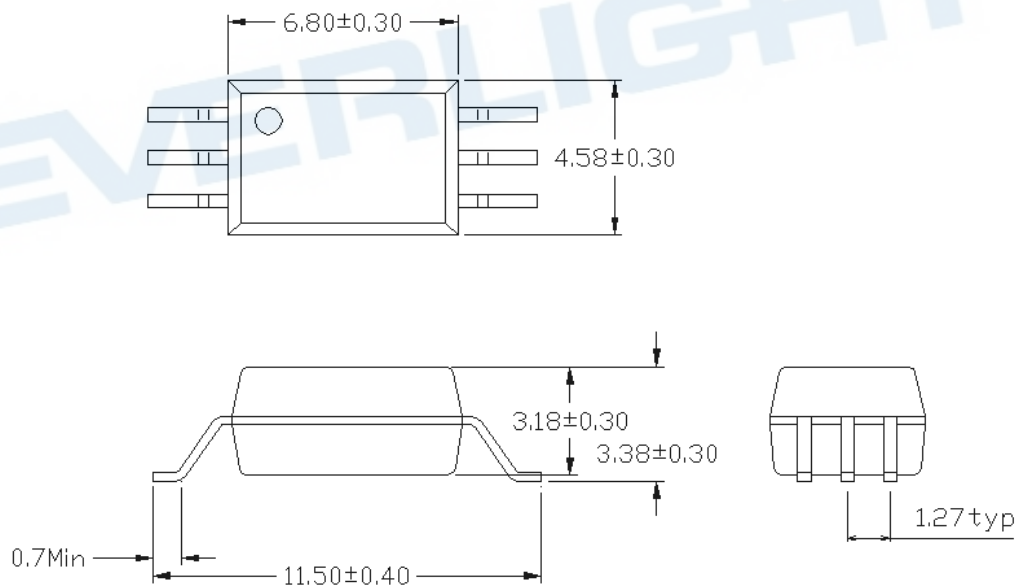
EVERLIGHT

Package Dimension
(Dimensions in mm)

P Type

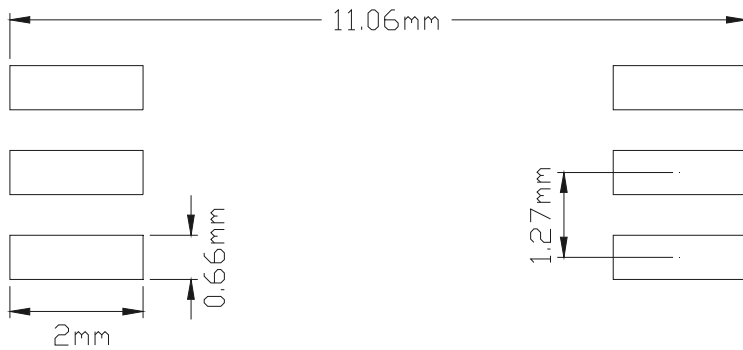


W Type

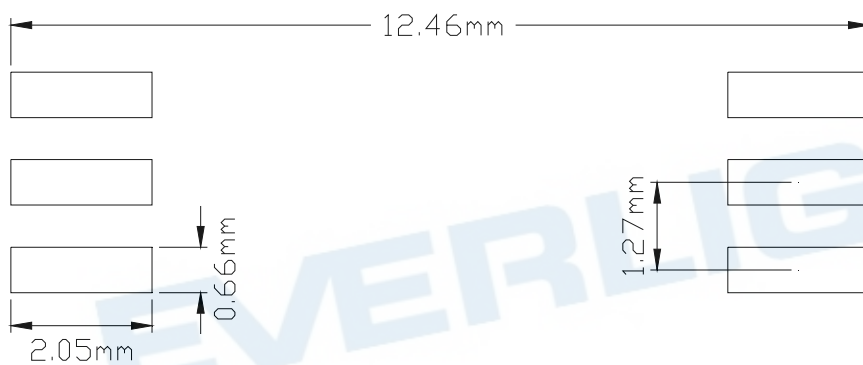


Recommended pad layout for surface mount leadform

For P Type:



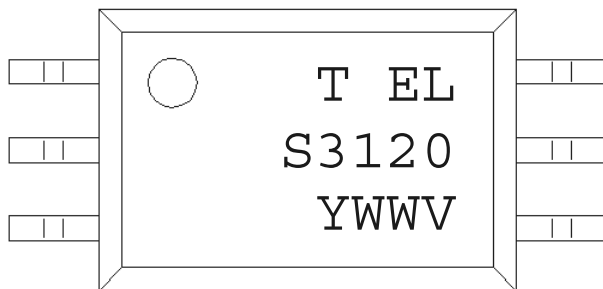
For W Type:



Notes.

Suggested pad dimension is just for reference only.
Please modify the pad dimension based on individual need.

Device Marking



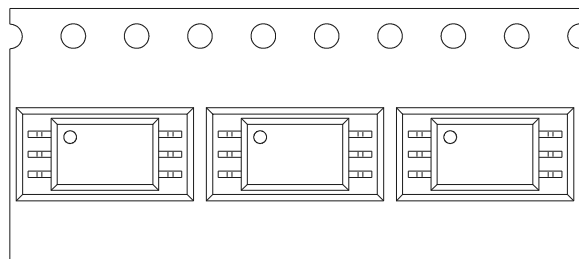
Notes

T	denotes Factory T : made in Taiwan
EL	denotes EVERLIGHT
S3120	denotes Device Number
Y	denotes 1 digit Year code
WW	denotes 2 digit Week code
V	denotes VDE (optional)

EVERLIGHT

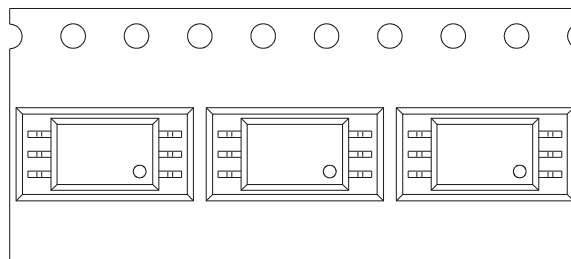
Tape & Reel Packing Specifications

Option TA



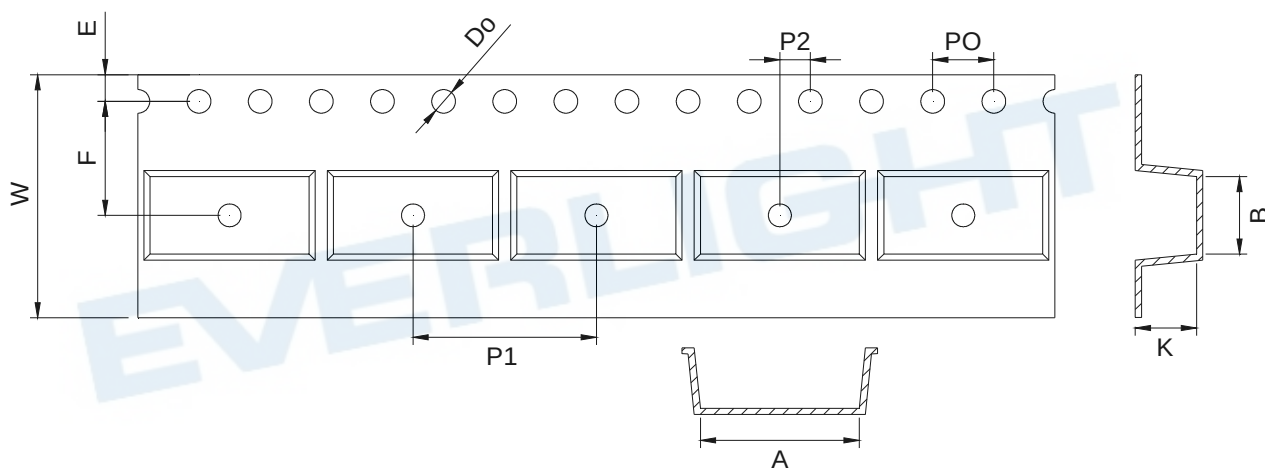
Direction of feed from reel

Option TB



Direction of feed from reel

Tape dimension

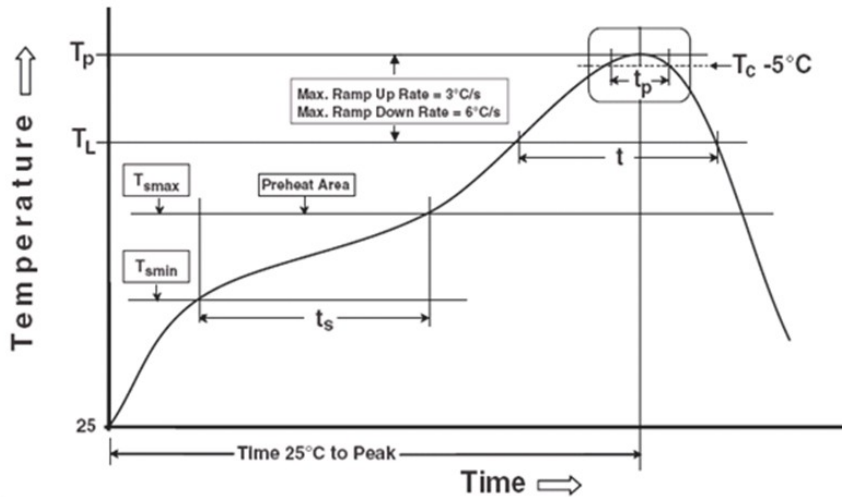


Dimension No.	A	B	Do	E	F	t
Dimension(mm) P	10.4 ± 0.2	4.9 ± 0.2	1.5 ± 0.1	1.75 ± 0.1	7.5 ± 0.1	0.4 ± 0.1
Dimension(mm) W	12.2 ± 0.2	4.9 ± 0.2	1.5 ± 0.1	1.75 ± 0.1	7.5 ± 0.1	0.4 ± 0.1
Dimension No.	PO	P1	P2	W	K	
Dimension(mm) P	4.0 ± 0.1	12.0 ± 0.1	2.0 ± 0.1	16.0 ± 0.3	3.7 ± 0.2	
Dimension(mm) W	4.0 ± 0.1	16.0 ± 0.1	2.0 ± 0.1	16.0 ± 0.3	3.7 ± 0.2	

Precautions for Use

1. Soldering Condition

1.1 (A) Maximum Body Case Temperature Profile for evaluation of Reflow Profile



Note:

Reference: IPC/JEDEC J-STD-020D

Preheat

Temperature min (T_{smin})	150 °C
Temperature max (T_{smax})	200°C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max

Other

Liquidus Temperature (T_L)	217 °C
Time above Liquidus Temperature (t_L)	60-100 sec
Peak Temperature (T_P)	260°C
Time within 5 °C of Actual Peak Temperature: $T_P - 5^\circ\text{C}$	30 s
Ramp- Down Rate from Peak Temperature	6°C /second max.
Time 25°C to peak temperature	8 minutes max.
Reflow times	3 times

DISCLAIMER

1. Above specification may be changed without notice. EVERLIGHT will reserve authority on material change for above specification.
2. The graphs shown in this datasheet are representing typical data only and do not show guaranteed values.
3. When using this product, please observe the absolute maximum ratings and the instructions for use outlined in these specification sheets. EVERLIGHT assumes no responsibility for any damage resulting from use of the product which does not comply with the absolute maximum ratings and the instructions included in these specification sheets.
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