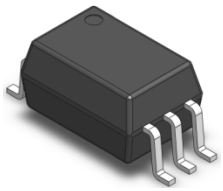
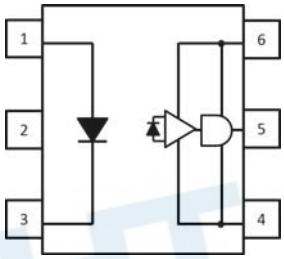
DATASHEET

# 6 PIN SDIP INTELLIGENT POWER and GATE DRIVE INTERFACE PHOTOCOUPLER
# ELS680-G series



Schematic




A 0.1μF bypass capacitor must be connected between pins 6 and 4

Pin Configuration
1: Anode
2: No Connection
3: Cathode
4: Gnd
5: $V_{out}$
6: $V_{CC}$

## Features

- Compliance Halogens Free
  ( Br < 900 ppm, Cl < 900 ppm, Br+Cl < 1500 ppm)
- Pb free and RoHS compliant
- Compliance with EU REACH.
- High isolation voltage between input and output (Viso=5000 Vrms )
- UL and cUL approved
- VDE approved
- NEMKO approved
- FIMKO approved
- SEMKO approved
- DEMKO approved
- CQC approved

## Description

The ELS680-G series devices each consists of an infrared emitting diode, optically coupled to a high speed integrated photo detector logic gate with a totem output. The totem pole output eliminates the need for a pull-up resistor and allows for a direct-drive Intelligent Power Module or gate drive. The devices are packaged in a 6-pin small DIP package.

## Applications

- IPM Interface Isolation
- Isolated IGBT/MOSFET Gate Drive
- AC and Brushless DC Motor Drives
- Industrial Inverters

## Truth Table

| Input | Output |
|---|---|
| H | H |
| L | L |

## Absolute Maximum Ratings (Ta=25°C) *1

| Parameter | | Symbol | Rating | Unit |
|---|---|---|---|---|
| Input | Forward current | $I_F$ | 25 | mA |
| | Reverse voltage | $V_R$ | 5 | V |
| | Power dissipation | $P_{IN}$ | 75 | mW |
| Output | Output current | $I_O$ | 60 | mA |
| | Supply voltage | $V_{CC}$ | 30 | V |
| | Power dissipation | $P_O$ | 270 | mW |
| Total Power Dissipation | | $P_{TOT}$ | 350 | mW |
| Isolation voltage *2 | | $V_{ISO}$ | 5000 | Vrms |
| Operating temperature | | $T_{OPR}$ | -40 ~ +100 | °C |
| Storage temperature | | $T_{STG}$ | -55 ~ +125 | °C |
| Soldering temperature *3 | | $T_{SOL}$ | 260 | °C |

Notes:
*1 Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this document. Exposure to absolute maximum ratings for extended periods of the time can adversely affect reliability. The absolute maximum Ratings are stress only $T_A$=25ºC unless otherwise specified.

*2 AC for 1 minute, R.H.= 40 ~ 60% R.H. In this test, pins 1, 2, 3 are shorted together, and pins 4, 5, 6 are shorted together.

*3 For 10 seconds.

## Electrical Characteristics (Ta=25°C, unless specified otherwise)

### Input

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Forward Voltage | $V_F$ | - | 1.5 | 1.8 | V | $I_F$=10mA |
| Reverse Voltage | $I_R$ | - | - | 10 | μA | $V_R$=5V |
| Input Capacitance | $C_{IN}$ | - | 60 | - | pF | $V_F$=0V, f=1MHz |

### Output

| Parameter | Symbol | Min | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| High Level Supply Current | $I_{CCH}$ | - | 0.9 | 3.2 | mA | $V_{CC}$=5.5V , $I_F$=10mA |
| Low Level Supply Current | $I_{CCL}$ | - | 0.9 | 3.2 | mA | $V_{CC}$=5.5V , $I_F$=0mA |
| Logic High Short Circuit Output Current | $I_{OSH}$ | - | - | -60 | mA | $V_{CC}$=5.5V, $I_F$=10mA, $I_O$=Open |
| Logic Low Short Circuit Output Current | $I_{OSL}$ | 60 | - | - | mA | $V_{CC}$=$V_O$=5.5V, $V_F$=0V |

## Transfer Characteristics (Ta=25°C, unless specified otherwise)

| Parameter | Symbol | Min | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| High Level Output Voltage | $V_{OH}$ | 4 | 4.5 | - | V | $V_{CC}$=4.5V, $I_F$=10mA, $I_O$=-0.4mA |
| Low Level Output Voltage | $V_{OL}$ | - | 0.1 | 0.5 | V | $V_{CC}$=4.5V, $I_F$=0mA, $I_O$=6.4mA |
| Input Threshold Current | $I_{FT}$ | - | 2.5 | 5 | mA | $V_{CC}$=4.5V |
| Input-Output Resistance | $R_{I-O}$ | - | $10^{12}$ | - | Ω | $V_{I-O}$=500V DC |
| Input-Output Capacitance | $C_{I-O}$ | - | 0.6 | - | pF | $V_{I-O}$=0V DC, f=1MHz |

## Switching Characteristics ($T_a$=25°C, $V_{CC}$=4.5V, $I_F$=10mA unless specified otherwise)

| Parameter | Symbol | Min | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Propagation Delay Time to Logic High (Fig.10) | $t_{PLH}$ | - | 140 | 350 | ns | $V_{CC}$=4.5V, $I_F$=10mA $T_A$=25°C |
| Propagation Delay Time to Logic Low (Fig.10) | $t_{PHL}$ | - | 130 | 350 | ns | $V_{CC}$=4.5V, $I_F$=10mA $T_A$=25°C |
| Pulse Width Distortion | $\|t_{PHL} - t_{PLH}\|$ | - | - | 250 | ns | $V_{CC}$=4.5V, $I_F$=10mA $T_A$=25°C |
| Output Rise Time (Fig.10) | tr | - | 9 | - | ns | $V_{CC}$=4.5V, $I_F$=10mA $T_A$=25°C |
| Output fall time (Fig.10) | tf | - | 6 | - | ns | $V_{CC}$=4.5V, $I_F$=10mA $T_A$=25°C |
| Common Mode Transient Immunity at Logic High (Fig.11) *4 | $CM_H$ | 10 | - | - | KV/μs | $V_{CM}$=1500Vp-p, $I_F$=7.5mA, $V_{CC}$=5V, $T_A$ =25°C |
| Common Mode Transient Immunity at Logic Low (Fig.11) *4 | $CM_L$ | 10 | - | - | KV/μs | $V_{CM}$=1500Vp-p, $I_F$=0mA, $V_{CC}$=5V, $T_A$ =25°C |

## Typical Electro-Optical Characteristics Curves

Figure 1. Low Level Output Voltage vs Ambient Temperature

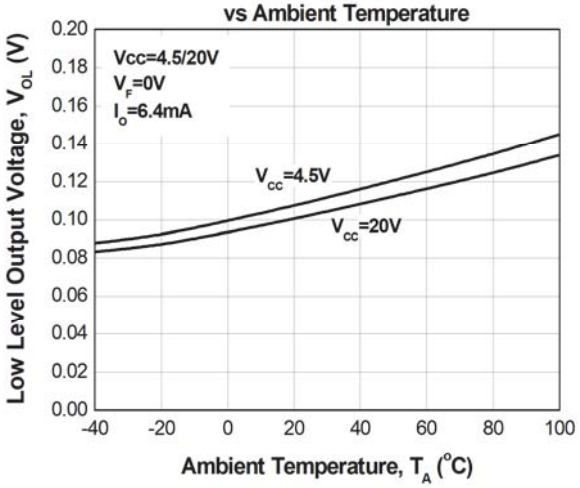



Figure 2. High Level Output Voltage vs Ambient Temperature

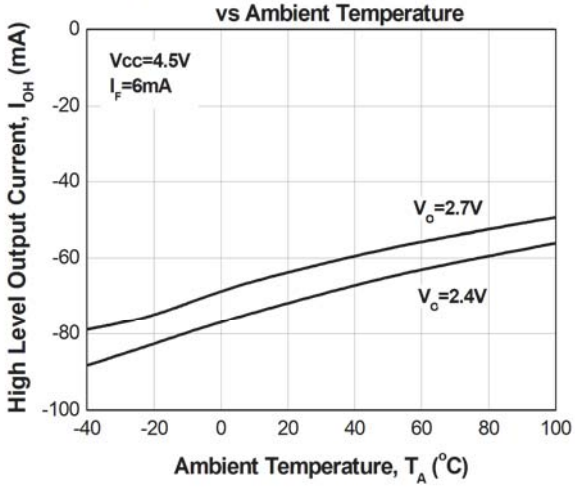



Figure 3. Output Voltage vs Input Current

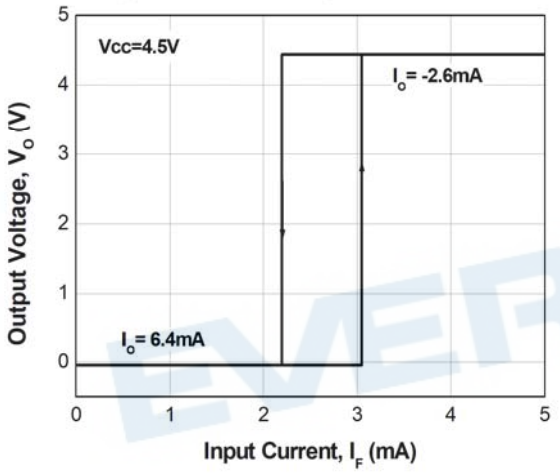



Figure 4. Forward Current vs Forward Voltage

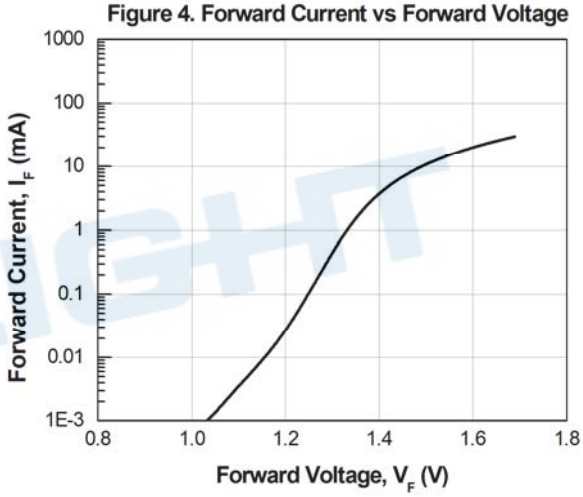



Figure 5. Propagation delay vs Ambient Temperature

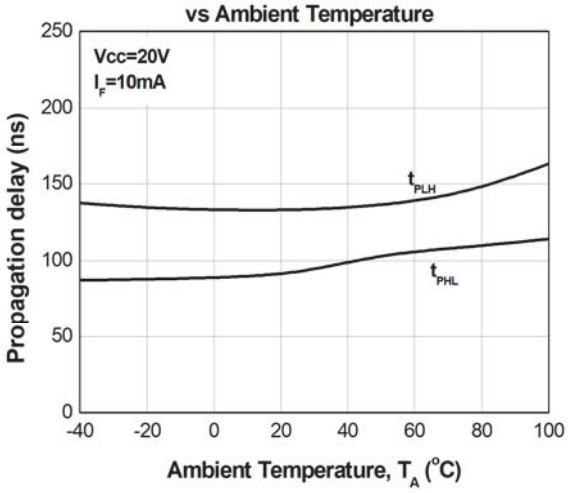



Figure 6. Output Voltage vs Supply Voltage

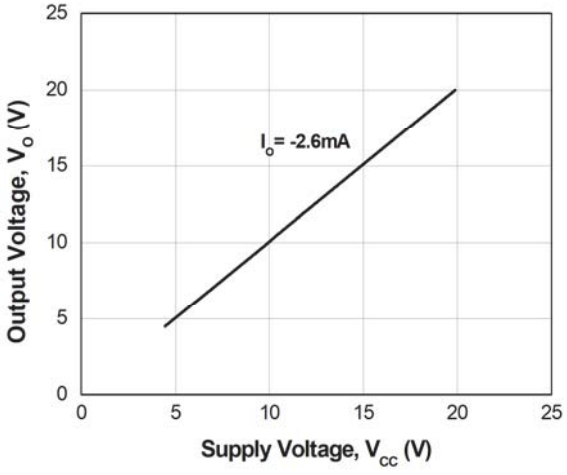


Figure 7. Propagation delay vs Supply Voltage

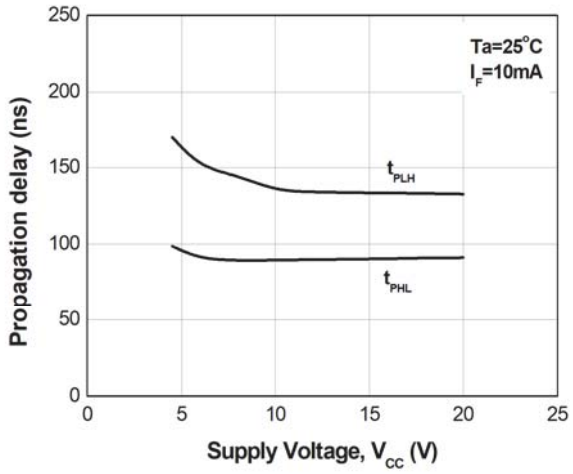



Figure 8. High Level Output Voltage vs Output Current

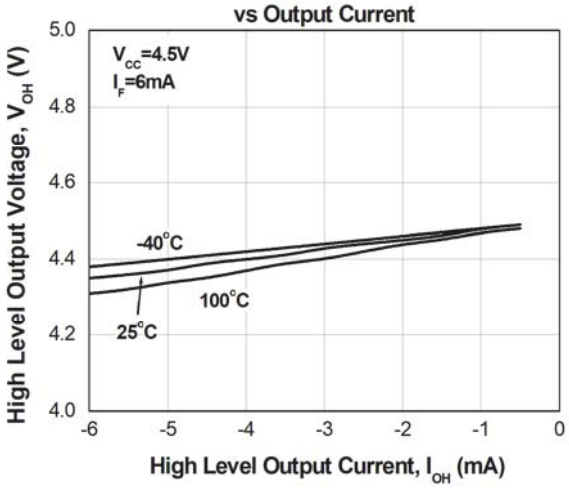



Figure 9. Low Level Output Voltage vs Low Current

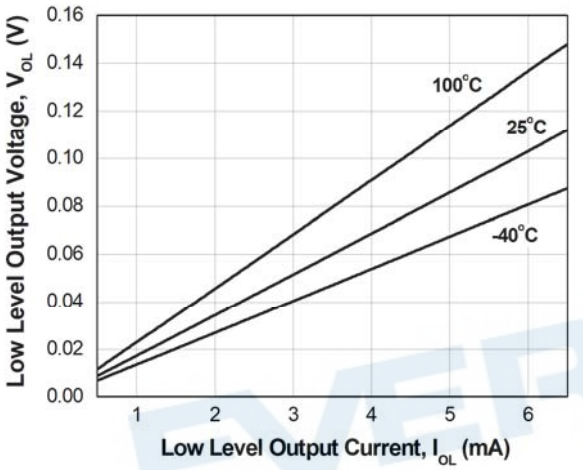


**Figure 10. Switching Time Test Circuit & Waveform** *5

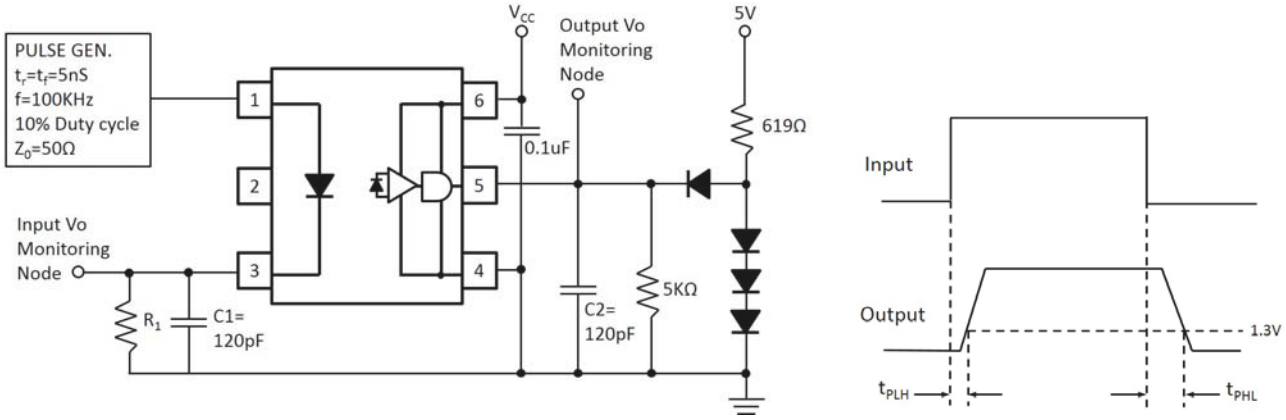
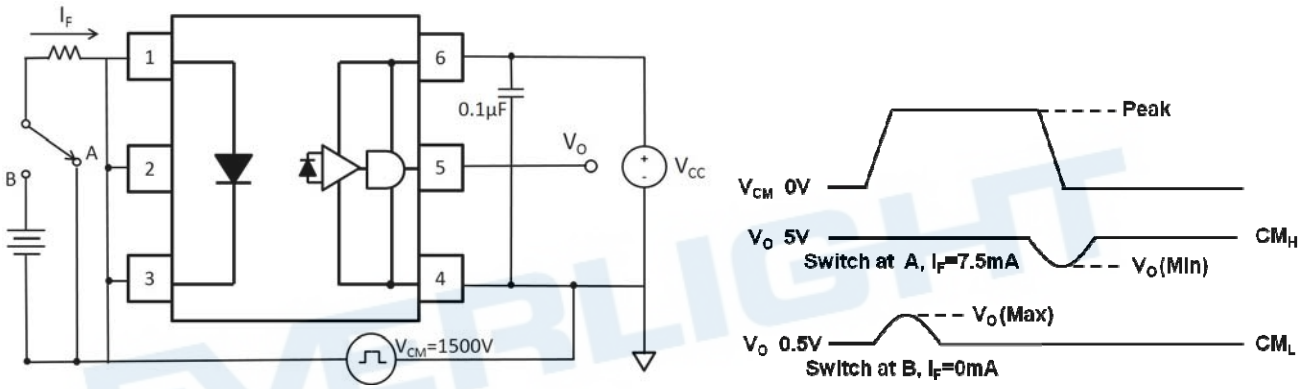



**Figure 11. Transient Immunity Test Circuit & Waveform**




Note:

*4 Common mode transient immunity in logic high level is the maximum tolerable (positive) dVcm/dt on the leading edge of the common mode pulse signal VCM, to assure that the output will remain in a logic high state (i.e., VO > 2.0V).
Common mode transient immunity in logic low level is the maximum tolerable (negative) dVcm/dt on the trailing edge of the common mode pulse signal, VCM, to assure that the output will remain in a logic low state (i.e., VO < 0.8V).

*5 The $V_{CC}$ supply must be bypassed by a 0.1μF capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package $V_{CC}$ and Gnd pins.

## Order Information

### Part Number

# ELS680X(Y) -VG

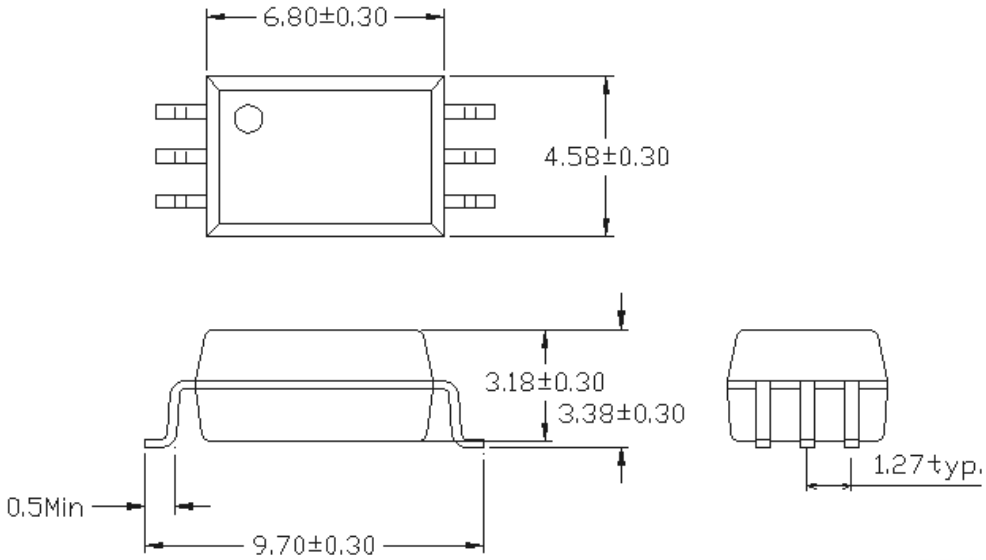
**Note**

EL = denotes EVERLIGHT
S680 = part no.
X = lead type(P)
Y = Tape and reel option (TA, TB)
V = VDE (optional)
G = Halogens free

| Option | Description | Packing quantity |
|---|---|---|
| P(TA) | Surface mount lead form + TA tape & reel option | 1000 units per reel |
| P(TB) | Surface mount lead form + TB tape & reel option | 1000 units per reel |

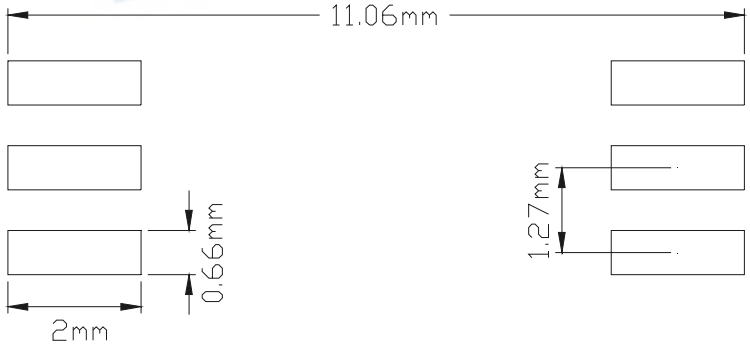
## Package Dimension
**(Dimensions in mm)**

**P Type**




## Recommended pad layout for surface mount leadform

**For P Type:**



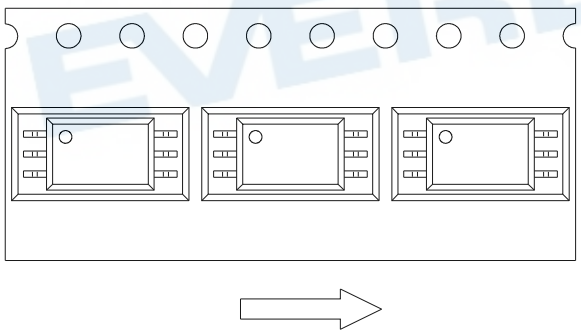
## Device Marking


**Notes**

| | |
|---|---|
| T | denotes Factory<br>T : made in Taiwan |
| EL | denotes EVERLIGHT |
| S680 | denotes Device Number |
| Y | denotes 1 digit Year code |
| WW | denotes 2 digit Week code |
| V | denotes VDE (optional) |

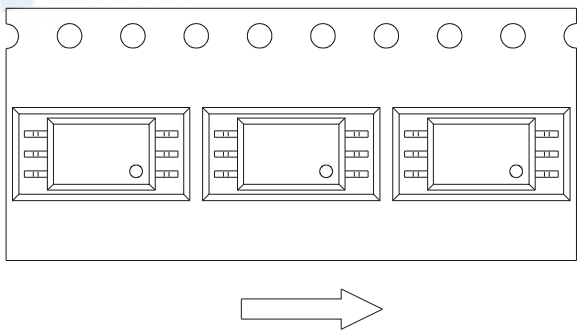
## Tape & Reel Packing Specifications

**Option TA**



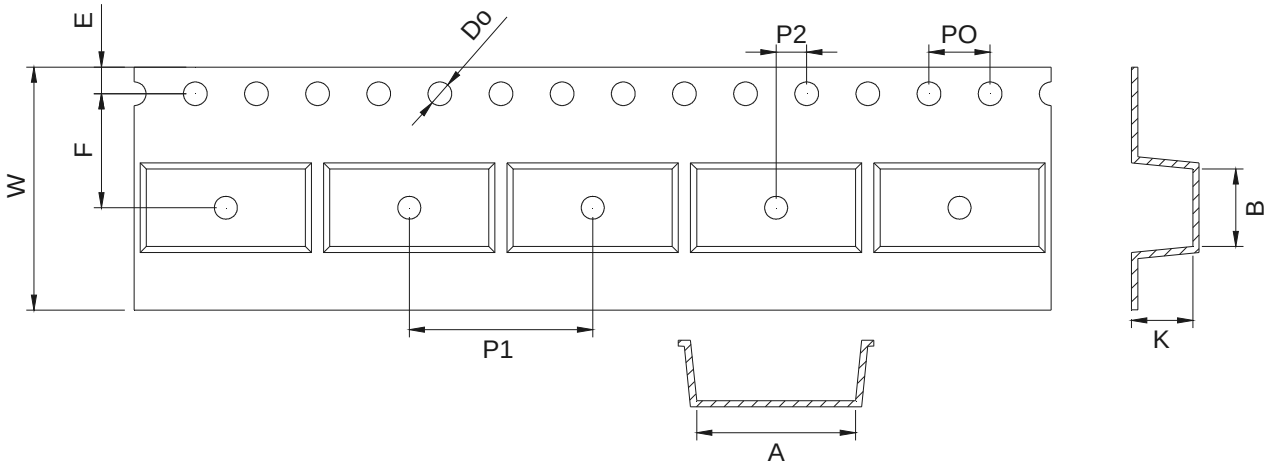
Direction of feed from reel

**Option TB**



Direction of feed from reel

## Tape dimension

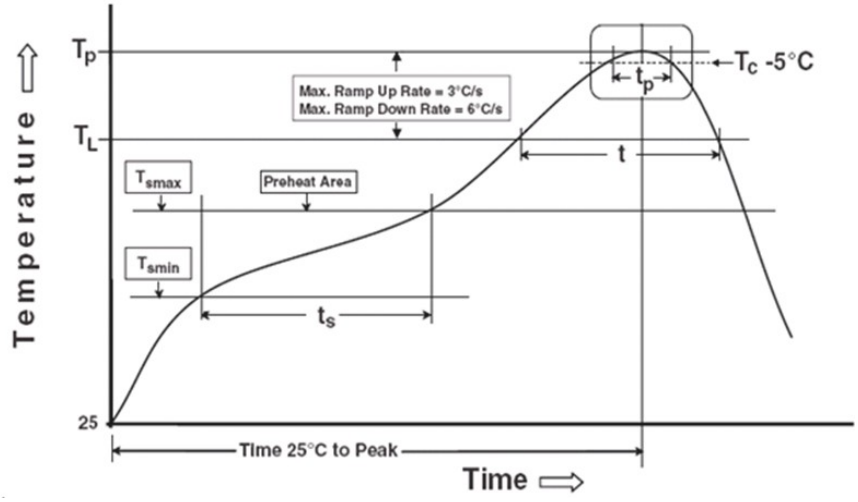



| Dimension No. | **A** | **B** | **Do** | **E** | **F** | **t** |
|---|---|---|---|---|---|---|
| Dimension(mm) P | 10.4 ± 0.1 | 5.1 ± 0.1 | 1.55 ± 0.1 | 1.75 ± 0.1 | 7.5 ± 0.1 | 0.4 ± 0.1 |
| Dimension No. | **PO** | **P1** | **P2** | **W** | **K** | |
| Dimension(mm) P | 4.0 ± 0.1 | 12.0 ± 0.1 | 2.0 ± 0.1 | 16.0 ± 0.3 | 4.0 ± 0.1 | |

## Precautions for Use

1. Soldering Condition

1.1 (A) Maximum Body Case Temperature Profile for evaluation of Reflow Profile




Note: Reference: IPC/JEDEC J-STD-020D

| | |
|---|---|
| **Preheat** | |
| Temperature min ($T_{smin}$) | 150 °C |
| Temperature max ($T_{smax}$) | 200°C |
| Time ($T_{smin}$ to $T_{smax}$) ($t_s$) | 60-120 seconds |
| Average ramp-up rate ($T_{smax}$ to $T_p$) | 3 °C/second max |
| **Other** | |
| Liquidus Temperature ($T_L$) | 217 °C |
| Time above Liquidus Temperature ($t_L$) | 60-100 sec |
| Peak Temperature ($T_P$) | 260°C |
| Time within 5 °C of Actual Peak Temperature: $T_P$ - 5°C | 30 s |
| Ramp- Down Rate from Peak Temperature | 6°C /second max. |
| Time 25°C to peak temperature | 8 minutes max. |
| Reflow times | 3 times |

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