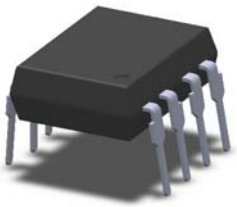
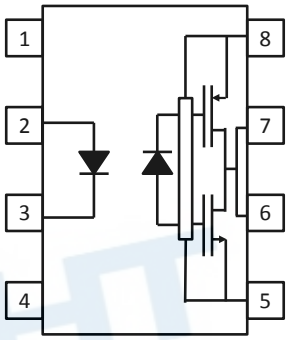
DATASHEET

# 8PIN WIDE BODY IGBT/MOSFET
# 2.5A Output Current GATE DRIVER PHOTOCOUPLER
# ELW3120(D) Series



Schematic




**Features:**

- Peak Output Current : $I_{OP}$ = 2.5A (max)
- Threshold Input Current: $I_{FLH}$ = 5 mA (max)
- High isolation voltage between input and output (Viso=5000 V rms )
- Pb free and RoHS compliant.
- UL and cUL approved
- VDE approved
- SEMKO approved
- NEMKO approved
- DEMKO approved
- FIMKO approved
- CQC approved

Pin Configuration
1, No Connection
2, Anode
3, Cathode
4. No Connection
5, $V_{EE}$
6, $V_{OUT}$
7, $V_{OUT}$
8, $V_{CC}$

A 0.1μF bypass capacitor must be connected between pins 8 and 5

## Description

The ELW3120 consists of an infrared light emitting diodes and integrated high gain, high-speed photo detectors. The device is housed in a 8 pin Wire body package.
The photo detector has an internal shield that provides a guaranteed common-mode transient immunity of ±20 kV/μs. It is suitable for direct gate driving circuit for IGBTs or power MOSFETs.

## Applications

- Isolated IGBT/Power MOSFET Gate Drive
- Uninterruptible power supply
- Inverters
- Home appliances, such as fan heaters, etc.

## Absolute Maximum Ratings (Ta=25°C)

| Parameter | | Symbol | Rating | Unit |
|---|---|---|---|---|
| Input | Forward current | $I_F$ | 25 | mA |
| | Pulse Forward Current*1 | $I_{FP}$ | 1 | A |
| | Reverse voltage | $V_R$ | 5 | V |
| Output | "H" Peak Output current | $I_{OPH}$ | 2.5 | A |
| | "L" Peak Output Current | $I_{OPL}$ | 2.5 | A |
| | Pear Output Voltage | $V_O$ | 30 | V |
| | Supply Voltage | $V_{CC}$ | 30 | V |
| Isolation voltage *2 | | $V_{ISO}$ | 5000 | V rms |
| Total Power Dissipation | | $P_T$ | 300 | mW |
| Operating temperature | | $T_{OPR}$ | -40 ~ +100 | °C |
| Storage temperature | | $T_{STG}$ | -55 ~ +125 | °C |
| Soldering temperature *3 | | $T_{SOL}$ | 260 | °C |

Notes:
*1 Pulse width ≤ 1μs, 300pps.
*2 AC for 1 minute, R.H.= 40 ~ 60% R.H. In this test, pins 1 to 4 are shorted together, and pins 5 to 8 are shorted together.
*3 For 10 seconds.

## Electro-Optical Characteristics

### Input

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Forward Voltage | $V_F$ | - | - | 1.8 | V | $I_F$ = 10mA |
| Reverse Voltage | $V_R$ | 5 | - | - | V | $I_R$ = 10μA |

### Output

| Parameter | Symbol | Min | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| High level supply current | $I_{CCH}$ | - | 1.8 | 3.2 | mA | $I_F$=10mA, $V_{CC}$=30V<br>$V_O$= Open |
| Low level supply current | $I_{CCL}$ | - | 2.2 | 3.2 | | $I_F$=0mA, $V_{CC}$=30V<br>$V_O$= Open |

### Transfer Characteristics

| Parameter | Symbol | Min | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| High Level Output Current*4 | $I_{OH}$ | - | - | -1 | A | $I_F$=10mA, $V_{CC}$=30V, $V_O$=$V_{CC}$-3V |
| | | - | - | -2.5 | | $I_F$=10mA, $V_{CC}$=30V, $V_O$=$V_{CC}$-6V |
| Low Level Output Current*4 | $I_{OL}$ | 1 | - | - | | $I_F$=0mA, $V_{CC}$=30V, $V_O$=$V_{EE}$ +3V |
| | | 2.5 | - | - | | $I_F$=0mA, $V_{CC}$=30V, $V_O$=$V_{EE}$ +6V |
| High Level Output Voltage | $V_{OH}$ | $V_{CC}$-0.5 | - | - | V | $I_F$=10mA, $V_{CC}$=30V, $I_O$=-100mA |
| Low Level Output Voltage | $V_{OL}$ | - | - | $V_{EE}$+0.5 | V | $I_F$=0mA, $V_{CC}$=30V, $I_O$=100mA |
| Input Threshold Current | $I_{FLH}$ | - | - | 5 | mA | $V_{CC}$=30V, $V_O$ >5V |
| Input Threshold Voltage | $V_{FHL}$ | 0.8 | - | - | V | $V_{CC}$=30V, $V_O$ <5V |
| Under Voltage Lockout Threshold | $V_{UVLO+}$ | 11.0 | - | 13.5 | V | $I_F$=10mA, $V_O$ >5V |
| Under Voltage Lockout Threshold | $V_{UVLO-}$ | 9.5 | - | 12.5 | V | $I_F$=10mA, $V_O$ <5V |

## Switching Characteristics

| Parameter | Symbol | Min | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Propagation delay time to output High level | $t_{PLH}$ | 50 | - | 400 | ns | $I_F$= 10mA<br>$V_{CC}$= 30V<br>$C_g$ = 10nF, $R_g$=10Ω,<br>f=10kHz, $T_A$=25°C<br>Duty Cycle=50%, |
| Propagation delay time to output Low level | $t_{PHL}$ | 50 | - | 400 | ns | |
| Pulse width distortion | $\lvert t_{PHL} - t_{PLH} \rvert$ | - | - | 150 | ns | |
| Propagation Delay Skew*5 | $t_{PSK}$ | - | - | 150 | ns | |
| Output rise time | $t_R$ | - | 80 | - | ns | |
| Output fall time | $t_F$ | - | 80 | - | ns | |
| Common Mode Transient Immunity at Logic High*6 | $CM_H$ | 20 | - | - | kV/μS | $I_F$ = 10mA , $V_{CC}$=30V, $T_A$=25°C $V_{CM}$=1500V |
| Common Mode Transient Immunity at Logic Low*7 | $CM_L$ | 20 | - | - | kV/μS | $I_F$ = 0mA , $V_{CC}$=30V, $T_A$=25°C $V_{CM}$=1500V |

**Notes:**

*4 Max. pulse width=10μS, max. duty cycle =1%

*5 Propagation delay skew is defined as the difference between the largest and smallest propagation delay times (i.e. $t_{PHL}$ or $t_{PLH}$) of multiple samples. Evaluations of these samples are conducted under identical test conditions (supply voltage, input current, temperature, etc).

*6 Common mode transient immunity at output high is the maximum tolerable negative dv/dt on the trailing edge of the common mode impulse signal, $V_{CM}$, to assure that the output will remain high (i.e. $V_O$>15.0V)

*7 Common mode transient immunity at output low is the maximum tolerable positive dv/dt on the leading edge of the common mode pulse signal, $V_{CM}$, to assure that the output will remain low (i.e. $V_O$<1.0V)

## Typical Electro-Optical Characteristics Curves

Figure 1. Forward Current vs Forward Voltage

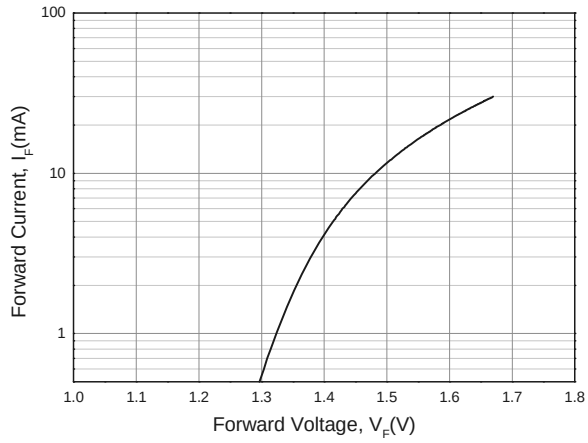



Figure 2. Threshold Input Current vs Ambient temperaturt

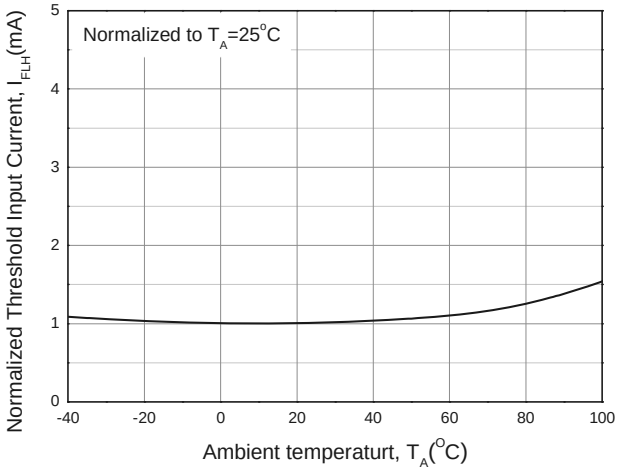



Figure 3. Low-level Supply Current vs Ambient temperaturt

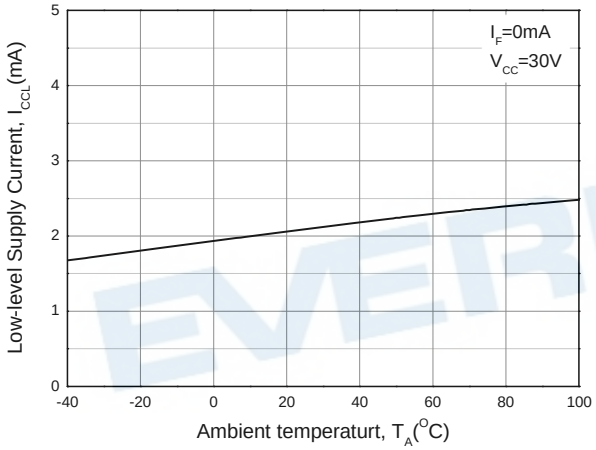



Figure 4. High-level Supply Current vs Ambient temperaturt

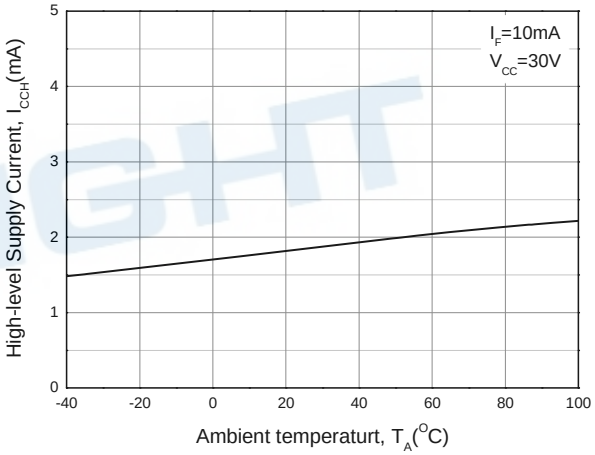



Figure 5. Low-level Output Voltage vs Ambient temperaturt

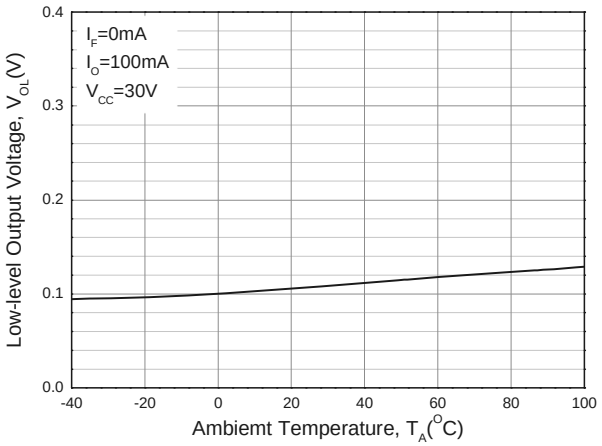



Figure 6. High-level Output Voltage vs Ambient temperaturt

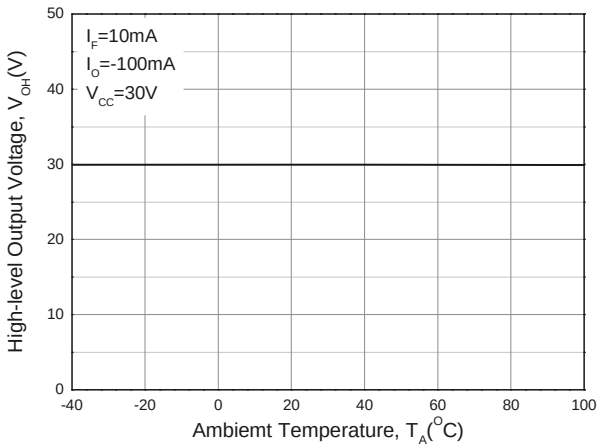


Figure 7. Low-level Output Voltage vs Peak low-level Output Current

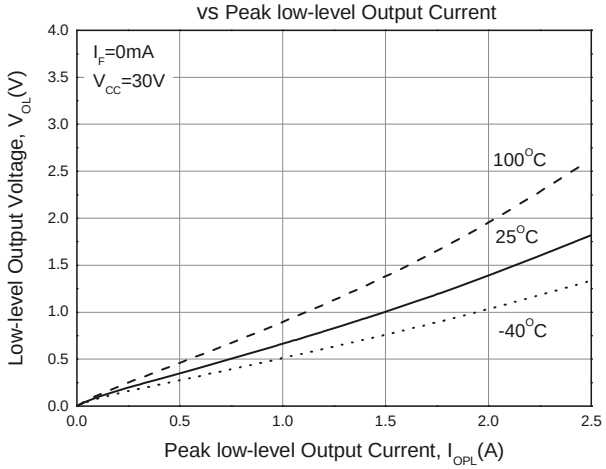



Figure 8. High-level Output Voltage Drop vs Peak low-level Output Current

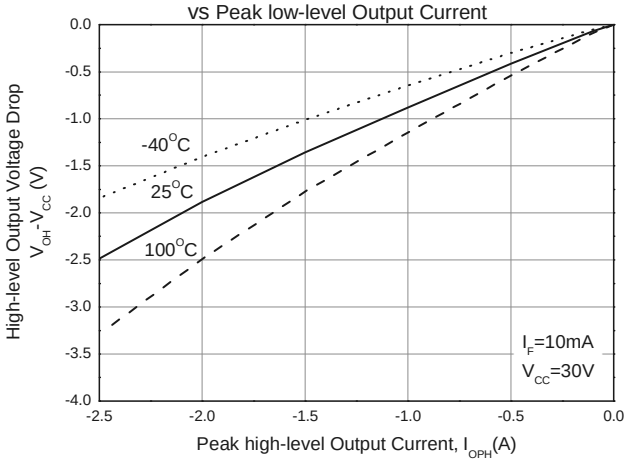



Figure 9. Propogation Delay Time vs Input Forward Current

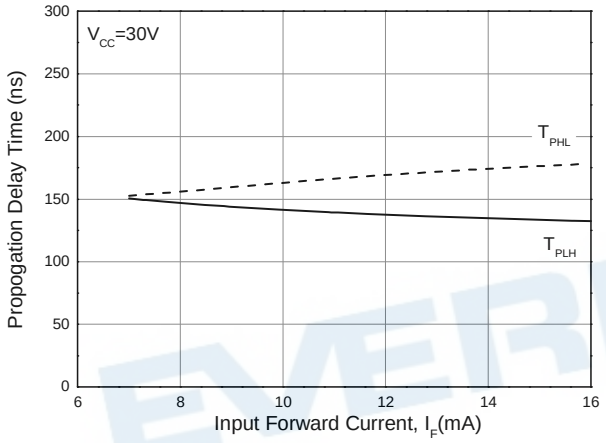



Figure 10. Propogation Delay Time vs Supply Voltage

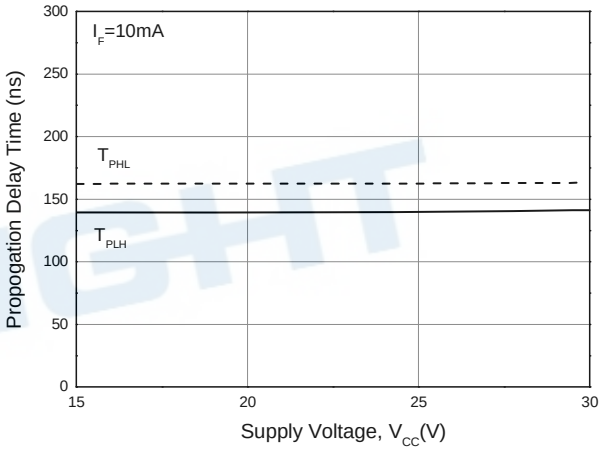



Figure 11. Propogation Delay Time vs Ambient Temperature

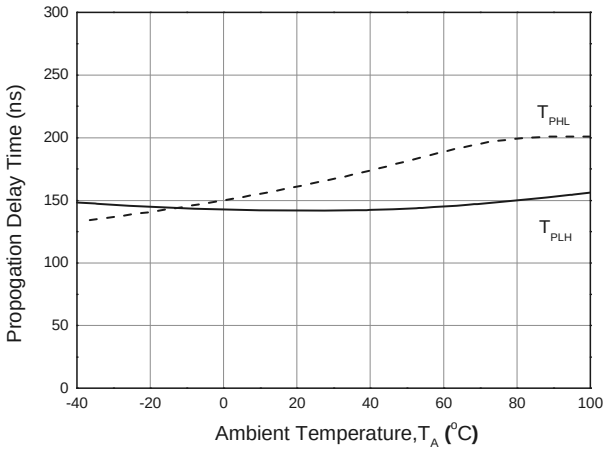


**Fig. 12 $I_{OH}$ Test circuit**

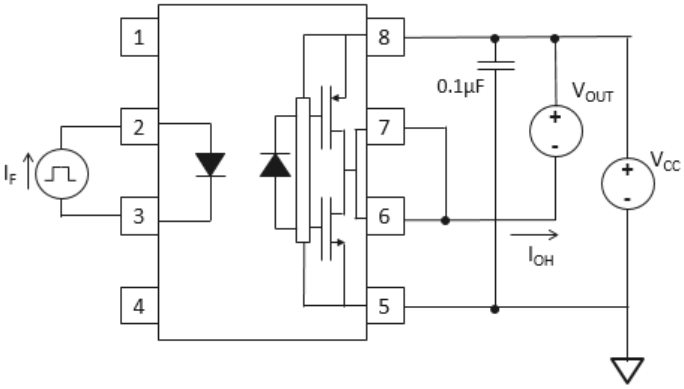



**Fig. 13 $I_{OL}$ Test circuit**

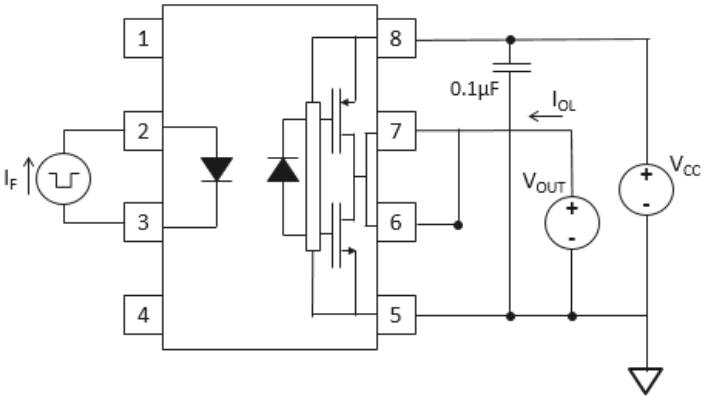



**Fig. 14 $V_{OH}$ Test circuit**

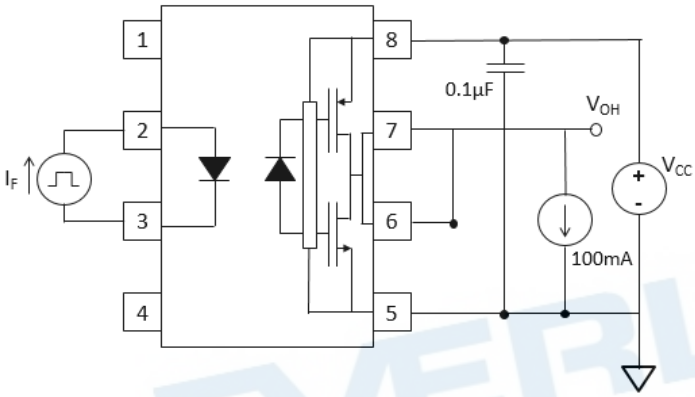



**Fig. 15 $V_{OL}$ Test circuit**

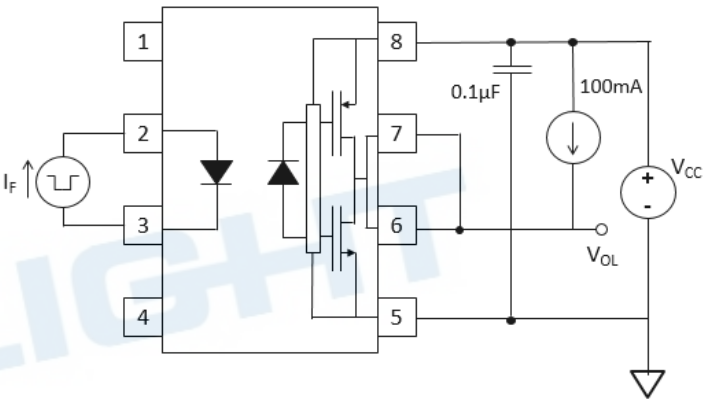



**Fig. 16 $I_{FHL}$ Test circuit**

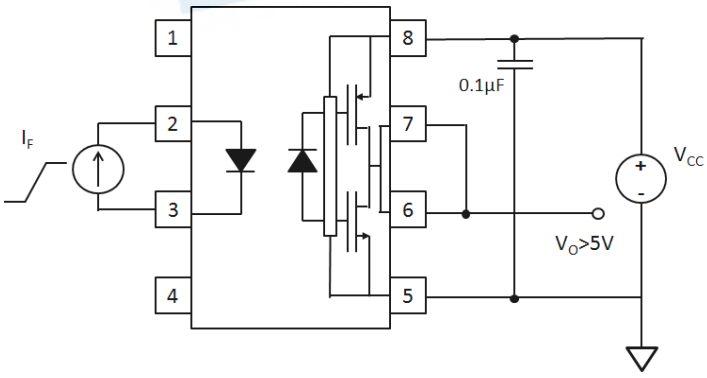
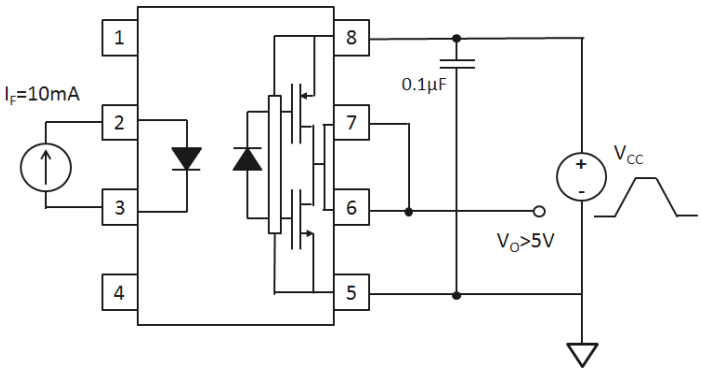
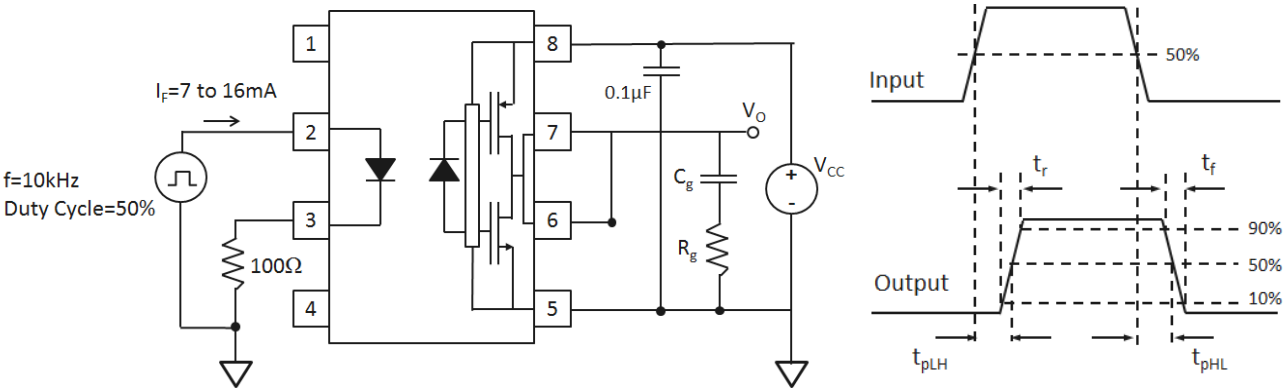


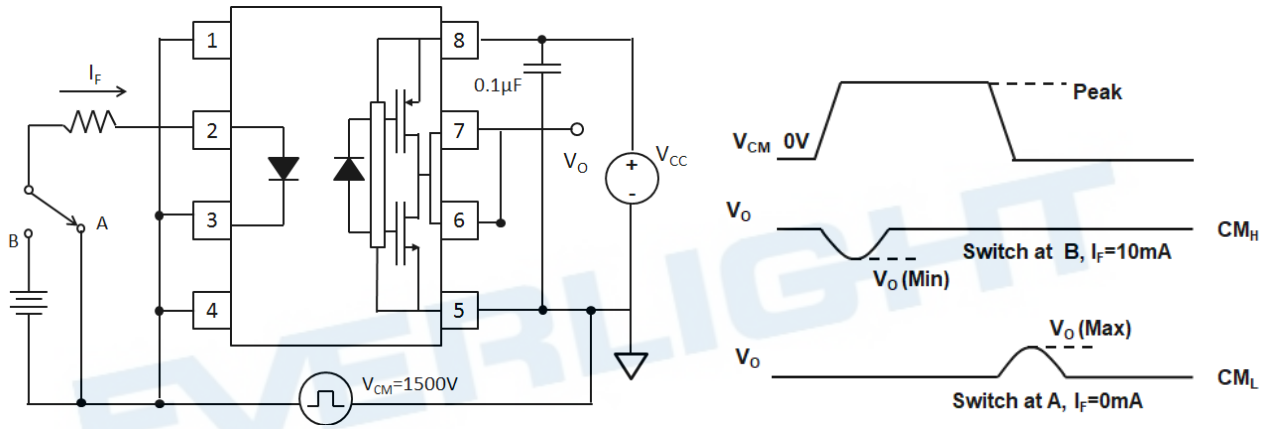

**Fig. 17 UVLO Test circuit**



## Fig. 18 Switching Time Test circuit




## Fig. 19 CMR Test circuit



## Order Information

### Part Number

# ELW3120X(Y)(D)-V

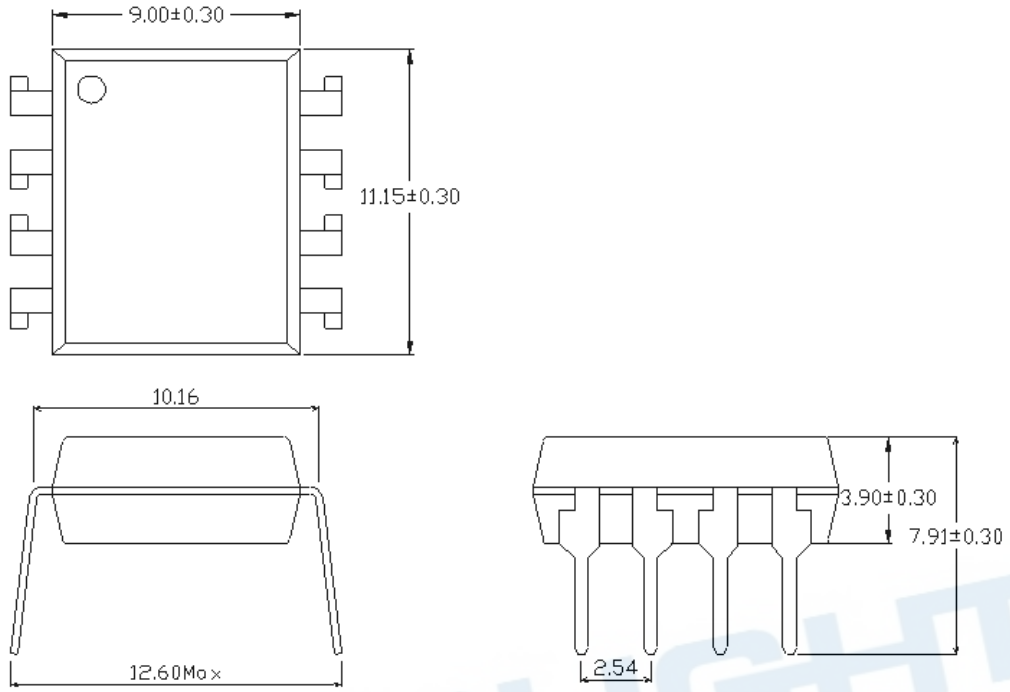
**Note**

| | | |
|---|---|---|
| EL | = | denotes EVERLIGHT |
| W3120 | = | part no. |
| X | = | Lead form option (S or none) |
| Y | = | Tape and reel option (TA, TB or none) |
| D | = | Customer Code |
| V | = | VDE safety (optional) |

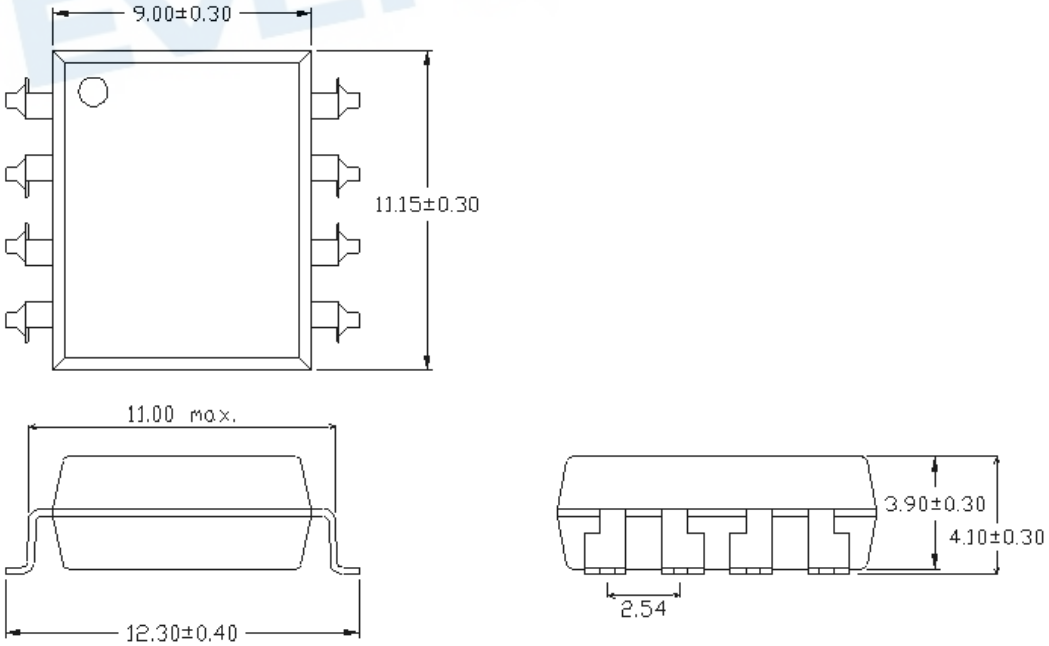
| Option | Description | Packing quantity |
|---|---|---|
| None | Standard | 45 units per tube |
| S (TA) | Surface mount lead form + TA tape & reel option | 500 units per reel |
| S (TB) | Surface mount lead form + TB tape & reel option | 500 units per reel |

## Package Dimension
**(Dimensions in mm)**

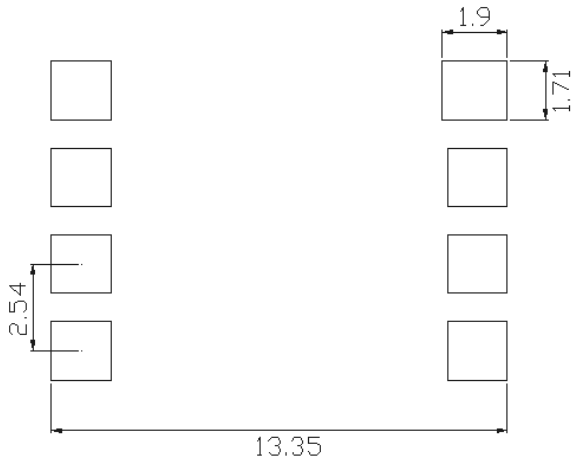
### Standard DIP Type




### Option S Type

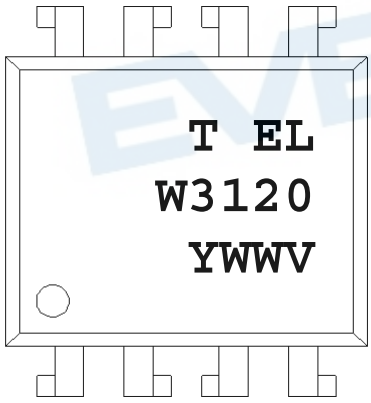


## Recommended Pad Layout for Surface Mount Leadform




Notes.
Suggested pad dimension is just for reference only.
Please modify the pad dimension based on individual need.

## Device Marking

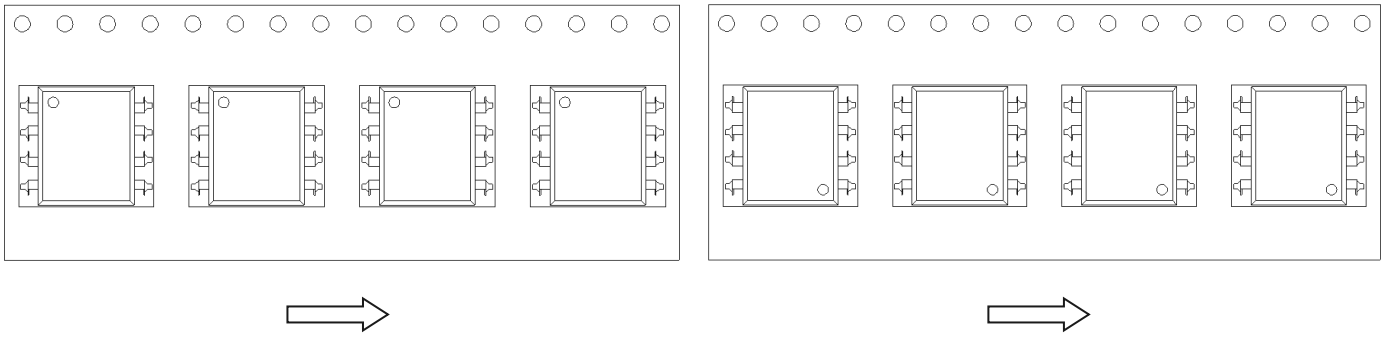



**Notes**

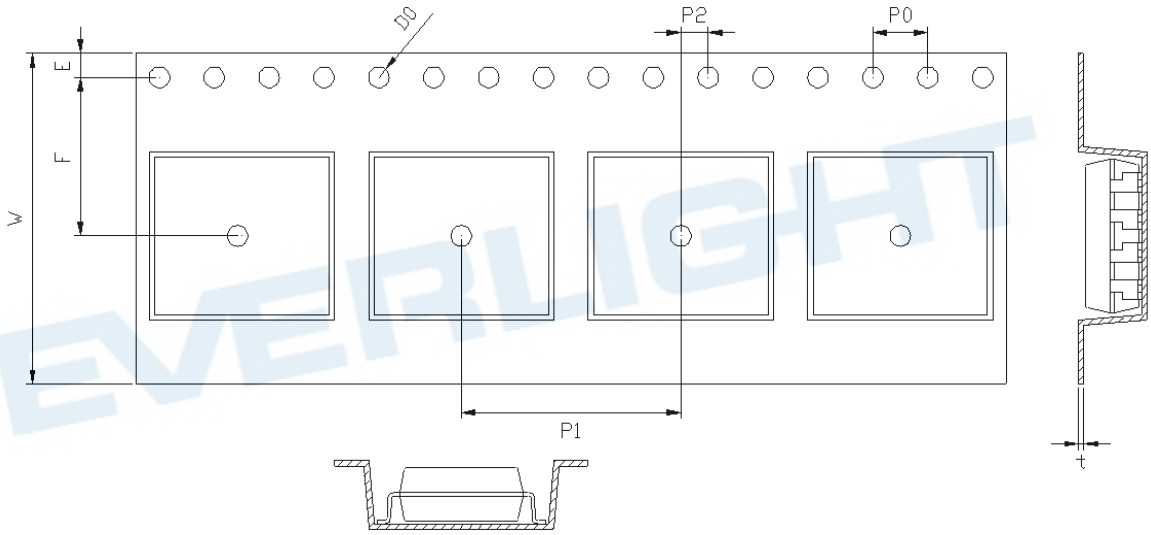
| | |
|---|---|
| T | denotes Factory<br>No code：made in China<br>T：made in Taiwan |
| EL | denotes EVERLIGHT |
| W3120 | denotes Device Number |
| Y | denotes 1 digit Year code |
| WW | denotes 2 digit Week code |
| V | denotes VDE (optional) |

## Tape & Reel Packing Specifications

**Option TA** **Option TB**



## Tape dimensions

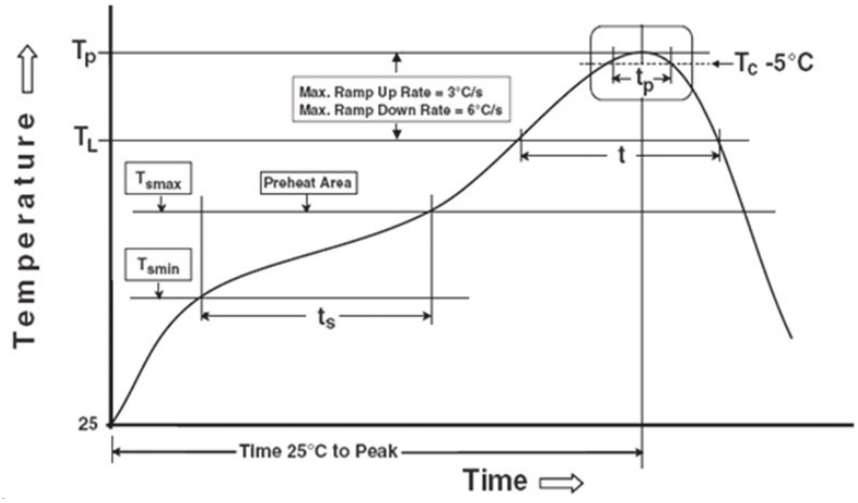



| Dimension No. | W | E | F | Do |
|---|---|---|---|---|
| Dimension(mm) | 24.00±0.3 | 1.75±0.1 | 11.5±0.1 | 1.5±0.1 |
| Dimension No. | Po | P1 | P2 | t |
| Dimension(mm) | 4.0±0.1 | 16.0±0.1 | 2.0±0.1 | 0.4±0.05 |

## Precautions for Use

1. Soldering Condition

1.1 (A) Maximum Body Case Temperature Profile for evaluation of Reflow Profile




Note: Reference: IPC/JEDEC J-STD-020D

| | |
|---|---|
| **Preheat** | |
| Temperature min ($T_{smin}$) | 150 °C |
| Temperature max ($T_{smax}$) | 200°C |
| Time ($T_{smin}$ to $T_{smax}$) ($t_s$) | 60-120 seconds |
| Average ramp-up rate ($T_{smax}$ to $T_p$) | 3 °C/second max |
| **Other** | |
| Liquidus Temperature ($T_L$) | 217 °C |
| Time above Liquidus Temperature ($t_L$) | 60-100 sec |
| Peak Temperature ($T_P$) | 260°C |
| Time within 5 °C of Actual Peak Temperature: $T_P$ -5°C | 30 s |
| Ramp- Down Rate from Peak Temperature | 6°C /second max. |
| Time 25°C to peak temperature | 8 minutes max. |
| Reflow times | 3 times |

## DISCLAIMER

1. Above specification may be changed without notice. EVERLIGHT will reserve authority on material change for above specification.
2. The graphs shown in this datasheet are representing typical data only and do not show guaranteed values.
3. When using this product, please observe the absolute maximum ratings and the instructions for use outlined in these specification sheets. EVERLIGHT assumes no responsibility for any damage resulting from use of the product which does not comply with the absolute maximum ratings and the instructions included in these specification sheets.
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