Industrial NC2780

Synchronous 34V Input Buck Switching Regulator (Controller)

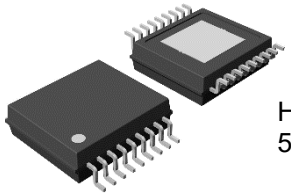
FEATURES

- Input Voltage (Maximum Rating): 4.0 V to 34 V (36 V)
- Start-Up Voltage: 4.5 V
- Output Voltage: 0.7 V to 5.3 V
- Feedback Voltage Tolerance: 0.64 V ± 1 %
- Quiescent Current: Typ. 15 μA (PFM at no load)
- Oscillation Frequency: 250 kHz to 1 MHz
- Soft-Start: 500 μs (When CSS is open)
  Can be optimized with external capacitance.
- Minimum On-Time: Typ. 100 ns
- Minimum OFF-Time: Typ. 120 ns
- Duty-Over: Oscillation Frequency × 1 to 1 / 4
- Operating mode: Auto switch mode, Force PWM mode, PLL sync mode
- Operating Temperature Range: -40 °C to 125 °C
- SSCG (Spread Spectrum) ※Option
- Power-Good
- Anti-Phase Clock Output
- Under Voltage Lockout (UVLO) Function: V_{CC} = Typ. 3.3 V
- Overvoltage Detection (OVD), Undervoltage Detection (UVD)
- Thermal Shutdown: Typ. 160 °C
- Output Overcurrent Protection: Hiccup mode/ Latch mode
- Short-Circuit Protection Function: SW to VIN or GND

GENERAL DESCRIPTION

The NC2780 is a CMOS-based controller-type buck switching regulator that operates using external high-side and low-side NMOSFETs. Equipped with a PFM function, it achieves high efficiency even at light loads, enabling low consumption in the system. Also, the switching frequency can be adjusted in the range of 250 kHz to 1 MHz by an external resistor.

This product (-D) is a highly reliable product that has undergone high temperature tests and reliability tests that are more severe than consumer products.

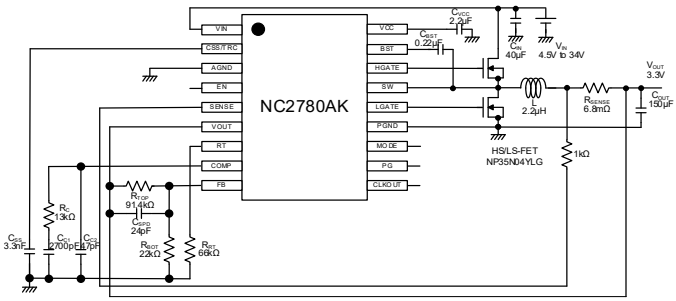


HSOP-18-AK
5.2 mm x 6.2 mm x 1.5 mm

APPLICATIONS

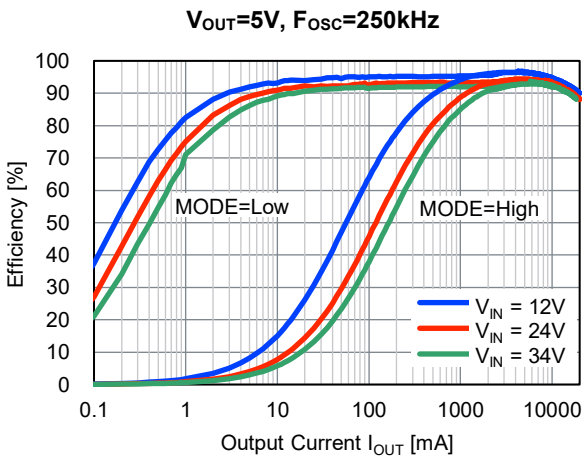
- Industrial equipments such as FAs and smart Meters.
- Equipments used under high-temperature conditions such as surveillance camera and vending machine.
- Equipments accompanied by self-heating such as motor and lighting.

TYPICAL APPLICATIONS



NC2780 TYPICAL APPLICATIONS

EFFICIENCY TYPICAL CHARACTERISTICS



PRODUCT NAME INFORMATION

NC2780 aa bbb c dd e

Description of Configuration

Composition	Item	Description
aa	Package Code	Indicates the package. AK: HSOP-18-AK
bbb	Output Voltage	Select the output voltage range and current limit threshold voltage.
c	Version	Select the Overcurrent Protection and SSCG.
dd	Packing	Taping direction. Refer to the packing specifications.
e	Grade	Indicates the quality grade.

Select the output voltage range and current limit threshold voltage.

bbb	Output Voltage Range	Current Limit Threshold Voltage (Typ.)	Reverse Current Limit Threshold Voltage (Typ.)
001	3.15V < V_{OUT} ≤ 5.3V	50mV	-25mV
002		70mV	-35mV
003		100mV	-50mV
101	0.7V ≤ V_{OUT} ≤ 3.15V	50mV	-25mV
102		70mV	-35mV
103		100mV	-50mV

Select the Overcurrent Protection and SSCG.

c	Overcurrent Protection	SSCG
A	Non-Latch Type Hiccup Mode	✓
B		-
C	Latch Mode	✓
D		-

Grade

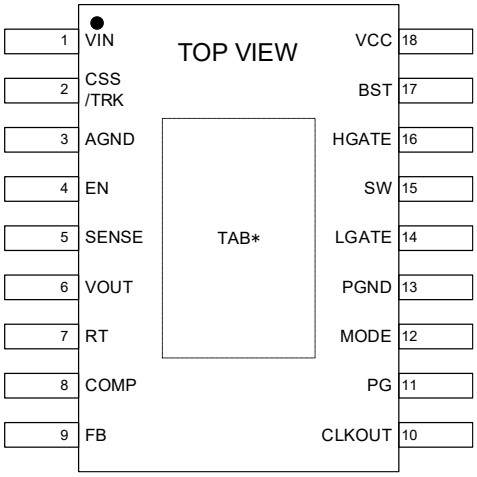
e	Applications	Operating Temperature Range	Test Temperature
D	Industrial Equipment and Social Infrastructures	-40°C to 125°C	25°C,125 °C

ORDER INFORMATION

PRODUCT NAME	PACKAGE	RoHS	HALOGEN-FREE	PLATING COMPOSITION	WEIGHT (mg)	QUANTITY (pcs/reel)
NC2780AK bbb c E2 e	HSOP-18-AK	✓	✓	Sn	81	1000

Click here for checking details.

PIN DESCRIPTIONS



NC2780 Pin Configuration

*TAB on the bottom of the package is the silicon substrate level.
Please be sure to connect to GND on the mounting board.

Pin No.	Pin Name	I/O	Description
1	VIN	I	Power Supply Input Pin
2	CSS/TRK	I	Soft-Start Adjustment Pin
3	AGND	—	Analog GND pin of internal circuit Be sure to connected to the PGND pin on the board.
4	EN	I	Enable Pin Input "Low" to this pin shuts down the IC. Input "High" to this pin enables the IC.
5	SENSE	I	Sense pin for inductor current Set the current value for current limit and reverse current limit by connecting a sense resistor.
6	VOUT	I	Power supply input pin for internal circuit / output voltage sense pin
7	RT	I	Timing Resistor pin to Program the Oscillator Frequency Connecting a resistor between the GND pin and this pin sets the switching frequency. Switching frequency range is from 250 KHz to 1 MHz.
8	COMP	O	Error Amplifier Phase Compensation Pin Connect a resistor and a capacitor for phase compensation.
9	FB	I	Feedback Input Pin Set the output voltage by connecting an external resistor.
10	CLKOUT	O	Clock Output Pin Outputs a pulse signal (Duty typ. 50%) whose phase is 180° different from the switching control signal inside the IC during PWM operation.
11	PG	O	Power-Good Output Pin NMOS open drain pin.
12	MODE	I	Mode Control Pin and External Clock Synchronization Input pin High: Forced PWM Control, Low: PWM/PFM Auto Switching Control, Clock input: PLL synchronization mode.
13	PGND	—	Power GND pin Be sure to connected to the AGND pin on the board.
14	LGATE	O	Gate Drive pin for Bottom(low-side) Synchronous N-Channel MOSFET.
15	SW	I	Switching Pin Connect the high-side MOSFET source, low-side MOSFET drain, and inductor.
16	HGATE	O	Gate Drive pin for Top(high-side) N-Channel MOSFET
17	BST	O	Bootstrapped Pin By connecting a capacitor (C_{BST}) between the BST and SW pin, the voltage between the BST and SW pin is controlled to Typ.5V. C_{BST} is charged from VCC.
18	VCC	O	Output pin of Internal 5V linear Regulator The control circuits of drive external MOSFETs are powered from this voltage source.

For details, refer to " *TYPICAL APPLICATION CIRCUIT* " and " *THEORY OF OPERATION* ".

ABSOLUTE MAXIMUM RATINGS

	Symbol	Ratings	Unit
VIN Pin Voltage	V_{IN}	-0.3 to 36	V
EN Pin Input Voltage	V_{EN}	-0.3 to V_{IN} + 0.3 ≤ 36	V
CSS/TRK Pin Voltage	$V_{CSS/TRK}$	-0.3 to V_{IN} + 0.3 ≤ 3	V
VOUT Pin Voltage	V_{OUT}	-0.3 to 6	V
SENSE Pin Voltage	V_{SENSE}	-0.3 to 6	V
RT Pin Voltage	V_{RT}	-0.3 to 3	V
COMP Pin Voltage	V_{COMP}	-0.3 to V_{CC} + 0.3 ≤ 6	V
FB Pin Voltage	V_{FB}	-0.3 to 3	V
VCC Pin Voltage	V_{CC}	-0.3 to 6	V
Output Current for VCC Pin		Internally limited	mA
BST Pin Voltage	V_{BST}	SW - 0.3 to SW + 6	V
HGATE Pin Voltage	V_{HGATE}	SW - 0.3 to BST	V
SW Pin Voltage	V_{SW}	-0.3 to V_{IN} + 0.3 ≤ 36	V
LGATE Pin Voltage	V_{LGATE}	-0.3 to 6	V
MODE Pin Voltage	V_{MODE}	-0.3 to 6	V
PG Pin Voltage	V_{PG}	-0.3 to 6	V
CLKOUT Pin Voltage	V_{CLKOUT}	-0.3 to V_{CC} + 0.3 ≤ 6	V
Junction Temperature Range [*1]	Tj	−40 to 150	°C
Storage Temperature Range	Tstg	−55 to 150	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

[*1] Please refer to "*THERMAL CHARACTERISTICS*" for the thermal resistance under our measurement board conditions.

THERMAL CHARACTERISTICS

Package	Parameter	Measurement Result	Unit
HSOP-18-AK	Thermal Resistance (θja)	32	°C / W
	Thermal Characterization Parameter (ψjt)	8	

θja : Junction-to-Ambient Thermal Resistance

ψjt : Junction-to-Top Thermal Characterization Parameter

The above values are reference data under measurement conditions based on JEDEC STD.51.

ELECTROSTATIC DISCHARGE RATINGS

	Conditions	Protection Voltage
HBM	C = 100pF, R = 1.5kΩ	±2000V
CDM		±1000V

ELECTROSTATIC DISCHARGE RATINGS

The electrostatic discharge test is done based on JESD47.
In the HBM method, ESD is applied using the power supply pin and GND pin as reference pins.

RECOMMENDED OPERATING CONDITIONS

	Symbol	Ratings	Unit
Input Voltage	V_{IN}	4.0 to 34	V
Operating Temperature Range	T_a	−40 to 125	°C
Output Voltage Range	V_{OUT}	0.7 to 5.3	V

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12 V, V_{EN} = V_{IN} unless otherwise specified.
For parameter that does not describe the temperature condition, the MIN / MAX value under the condition of −40 °C ≤ T_a ≤ 125 °C is described.

Parameter		Symbol	Conditions	MIN	TYP	MAX	Unit
Start-Up Voltage		V_{START}		-	-	4.5	V
VCC Pin Voltage (VCC - AGND)		V_{CC}	V_{FB} = 0.672 V	4.9	5.1	5.3	V
Shutdown Current		I_{SD}	V_{IN} = 34 V, V_{EN} = 0 V	-	3	21	μA
Quiescent Current 1 at Switching Stop in PWM Mode	NC2780AK0xxx	I_{Q1}	V_{FB} = 0.672 V, V_{MODE} = 5 V, V_{OUT} = V_{SENSE} = V_{SW} = 5 V	-	1.0	1.5	mA
	NC2780AK1xxx		V_{FB} = 0.672 V, V_{MODE} = 5 V, V_{OUT} = V_{SENSE} = V_{SW} = 1.5 V	-	1.6	2.1	
Quiescent Current 2 at Switching Stop in PFM Mode	NC2780AK0xxx	I_{Q2}	V_{FB} = 0.672 V, V_{MODE} = 0 V, V_{OUT} = V_{SENSE} = V_{SW} = 5 V	-	15	75	μA
	NC2780AK1xxx		V_{FB} = 0.672 V, V_{MODE} = 0 V, V_{OUT} = V_{SENSE} = V_{SW} = 1.5 V	-	45	145	
UVLO Release Voltage		$V_{UVLOREL}$	V_{CC} Rising	3.85	4.0	4.2	V
UVLO Detection Voltage		$V_{UVLODET}$	V_{CC} Falling	3.1	3.3	3.4	V
FB Pin Voltage		V_{FB}	T_a = 25 °C	0.6336	0.64	0.6464	V
			-40 °C ≤ T_a ≤ 125 °C	0.6272		0.6528	V
Oscillation Frequency 0		f_{OSC0}	R_{RT} = 135 kΩ	225	250	275	kHz
Oscillation Frequency 1		f_{OSC1}	R_{RT} = 32 kΩ	900	1000	1100	kHz
Minimum OFF Time		t_{OFF}	V_{IN} = 5 V, V_{OUT} = 5 V	-	120	190	ns
Minimum ON Time		t_{ON}	V_{IN} = 5 V, V_{OUT} = 0.7 V	-	100	120	ns
Synchronizing Frequency		f_{SYNC}	f_{OSC} as the reference	f_{osc}×0.5	-	f_{osc}×1.5	kHz
				250	-	1000	kHz
Soft-Start Time 1		t_{SS1}	CSS/TRK = OPEN	0.4	-	0.75	ms
Soft-Start Time 2		t_{SS2}	C_{SS} = 4.7 nF	1.4	-	2.0	ms
Charge Current for Soft-Start Pin		I_{TSS}	$V_{CSS/TRK}$ = 0 V	1.8	2	2.2	μA
CSS/TRK Pin Voltage at End of Soft-Start		V_{SSEND}		V_{FB}	V_{FB} + 0.03	V_{FB} + 0.06	V
Discharge Resistance for CSS/TRK Pin		R_{ONDIS_CSS}	V_{IN} = 4.5 V, V_{EN} = 0 V, $V_{CSS/TRK}$ = 3 V	2.0	3.0	5.0	kΩ

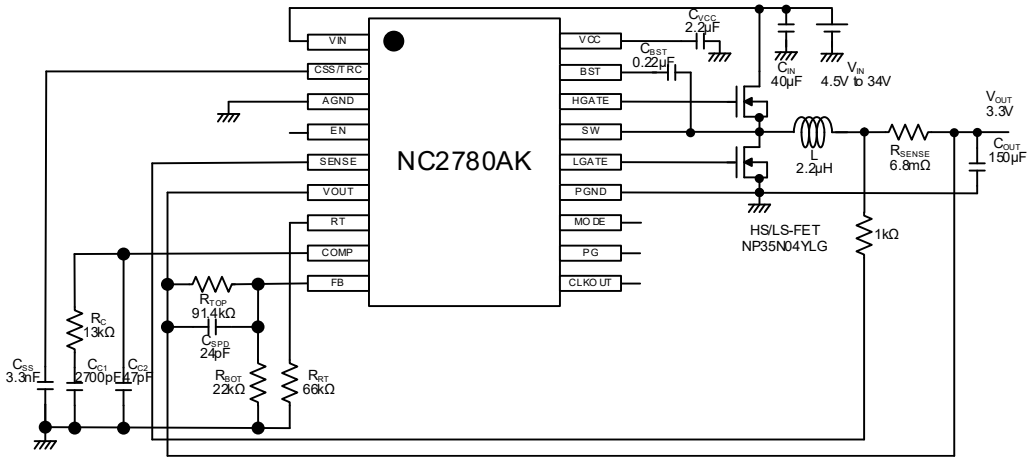
All electrical characteristic parameters that specify the minimum and maximum specifications are tested under the condition of $T_j \approx T_a$ = 25 °C / 125 °C

V_{IN} = 12 V, V_{EN} = V_{IN} unless otherwise specified.
For parameter that do not describe the temperature condition, the MIN / MAX value under the condition of −40 °C ≤ T_a ≤ 125 °C is described.

Parameter		Symbol	Conditions	MIN	TYP	MAX	Unit
On-resistance of Pull-up MOSFET (HGATE Pin)		$R_{UPHGATE}$	(BST - SW) = 5 V	-	2.5	7.0	Ω
On-resistance of Pull-down MOSFET (HGATE Pin)		$R_{DOWNHGATE}$	(BST - SW) = 5 V	-	1.5	5.0	Ω
On-resistance of Pull-up MOSFET (LGATE Pin)		$R_{UPLGATE}$		-	4.0	8.5	Ω
On-resistance of Pull-down MOSFET (LGATE Pin)		$R_{DOWNLGATE}$		-	1.5	5.0	Ω
Current Limit Threshold Voltage (SENSE - VOUT)	NC2780AKx01x	V_{ILIMIT}	MODE = “High”	40	50	60	mV
	NC2780AKx02x			60	70	80	mV
	NC2780AKx03x			90	100	110	mV
Reverse Current Sense Threshold (SENSE - VOUT)	NC2780AKx01x	$V_{IREVLIMIT}$	MODE = “High”	-35	-25	-15	mV
	NC2780AKx02x			-45	-35	-25	mV
	NC2780AKx03x			-60	-50	-40	mV
SW Short to GND Detector Threshold Voltage (VIN - SW)		$V_{SWSHORTDET}$		0.325	0.43	0.525	V
SW Short to VCC Detector Threshold Voltage (SW - PGND)		$V_{SWSHORTDET}$		0.310	0.43	0.535	V
EN Pin “High” Input Voltage		V_{ENH}		1.3	-	-	V
EN Pin “Low” Input Voltage		V_{ENL}		-	-	1.1	V
EN Pin “High” Input Current		I_{ENH}	V_{IN} = 34 V, V_{EN} = 34 V	0.20	-	2.45	μA
EN Pin “Low” Input Current		I_{ENL}	V_{IN} = 34 V, V_{EN} = 0 V	-1.00	0	1.00	μA
FB Pin “High” Input Current		I_{FBH}	V_{IN} = 34 V, V_{FB} = 3 V	-0.1	0	0.1	μA
FB Pin “Low” Input Current		I_{FBL}	V_{IN} = 34 V, V_{FB} = 0 V	-0.1	0	0.1	μA
MODE “High” Input Voltage		V_{MODEH}		1.35	-	-	V
MODE “Low” Input Voltage		V_{MODEL}		-	-	0.74	V
MODE “High” Input Current		I_{MODEH}	V_{IN} = 34 V, V_{MODE} = 6 V	1.00	-	6.80	μA
MODE “Low” Input Current		I_{MODEL}	V_{IN} = 34 V, V_{MODE} = 0 V	-1.0	0	1.0	μA
CLKOUT Pin “High” Output Voltage		$V_{CLKOUTH}$	CLKOUT = Hi - Z	4.7	-	VCC	V
CLKOUT Pin “Low” Output Voltage		$V_{CLKOUTL}$	CLKOUT = Hi - Z	0	-	0.1	V
PG Pin “Low” Output Voltage		V_{PGOFF}	V_{IN} = 4.0 V, I_{PG} = 1 mA	-	0.26	0.54	V
PG Pin Leakage Current		I_{PGOFF}	V_{IN} = 34 V, V_{PG} = 6 V	-0.10	0	0.10	μA
FB Pin OVD Threshold Voltage		$V_{FBOVDDET}$	V_{FB} Rising	0.680	V_{FB}×1.10	0.740	V
		$V_{FBOVDREL}$	V_{FB} Falling	0.664	V_{FB}×1.07	0.712	V
FB Pin UVD Threshold Voltage		$V_{FBUVDDET}$	V_{FB} Falling	0.556	V_{FB}×0.90	0.604	V
		$V_{FBUVDREL}$	V_{FB} Rising	0.574	V_{FB}×0.93	0.628	V
Trans Conductance Amplifier		gm (EA)	V_{COMP} = 1.5 V	0.35	1	1.55	mS

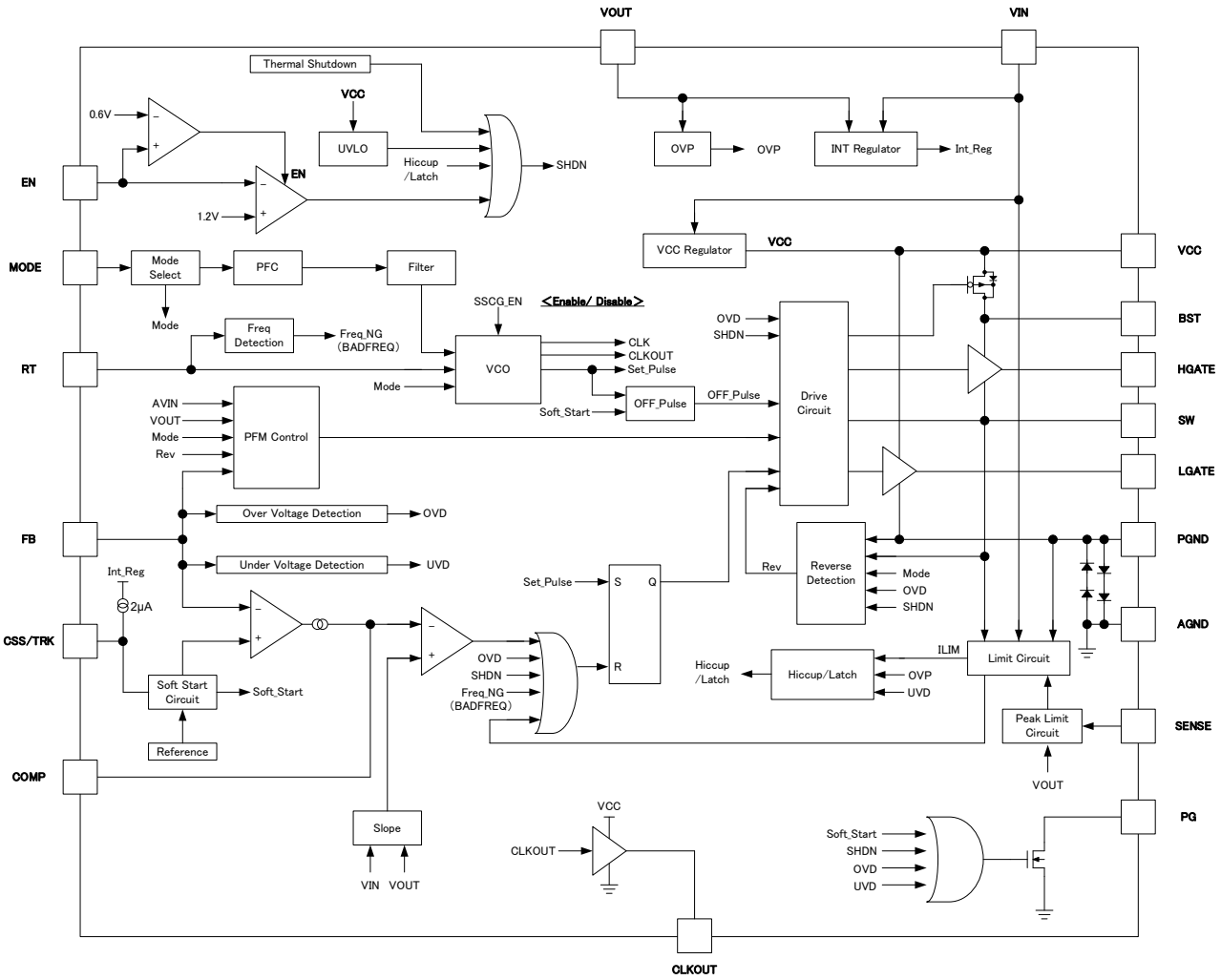
All electrical characteristic parameters that specify the minimum and maximum specifications are tested under the condition of $T_j \approx T_a$ = 25 °C / 125 °C

TYPICAL APPLICATION CIRCUIT



NC2780AK Typical Application Circuit

BLOCK DIAGRAMS



NC2780 Block Diagram

THEORY OF OPERATION

● Forced PWM Mode and PFM Mode

The output voltage control methods are selectable between the PWM / PFM auto-switching mode and the forced PWM mode by using the MODE pin.

Forced PWM Mode

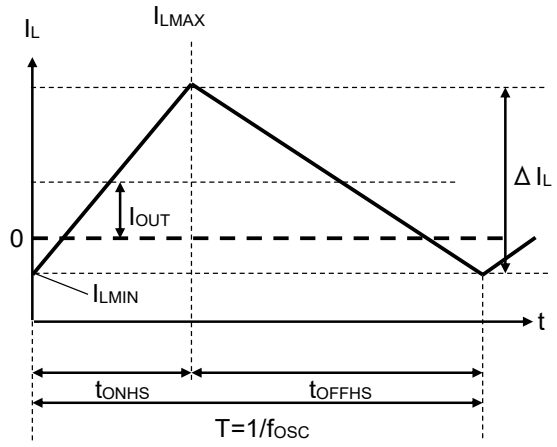
Forced PWM mode is selected when setting the MODE pin to “High”. This mode can reduce the output noise, since the frequency is fixed during light load conditions. Thus, I_{LMIN} becomes less than "0" when I_{OUT} is less than ΔI_L / 2. That is, the electric charge, which is charged to C_{OUT}, is discharged via MOSFET for the durations – when I_L reaches ”0” from I_{LMIN} during the t_{ONHS} periods and when I_L reaches I_{LMIN} from ”0” during t_{OFFHS} periods. But, pulses are skipped to prevent the overvoltage when high-side MOSFET is set to ON under the condition that the output voltage being more than the set output voltage.

PFM Mode

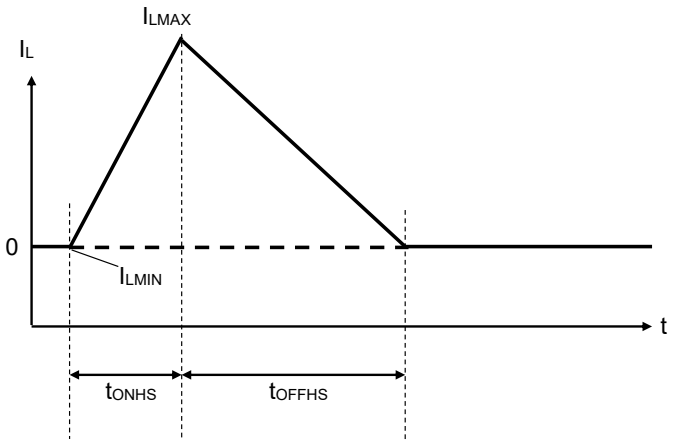
PWM / PFM auto-switching mode is selected when setting the MODE pin to “Low”. This mode can automatically switch from PWM to PFM to achieve a high-efficiency during light load conditions. By the PFM mode architecture, the high-side MOSFET is turned on for t_{ON} x 1.54 (typ) at the PWM mode under the same condition as the PFM mode when the FB pin voltage drops below the internal reference voltage (Typ.0.64 V). After the On-time, the high-side MOSFET is turned off and the low-side MOSFET is turned on. When the inductor current of 0 A is detected, the low-side MOSFET is turned off and the switching operation is stopped (Both of hi- and low-side MOSFETs are OFF). The switching operation restarts when the FB pin voltage becomes less than 0.64 V.

PWM/PFM auto-switching mode switches between PWM mode and PFM mode depending on the load current. When this product detects that the inductor current has become 0A for 16 consecutive cycles during light load, it switches from PWM mode to PFM mode. Also, if the load increases and the high-side MOSFET turns on before detecting 0A of inductor current, the PFM mode will switch to PWM mode.

The On-time at the PWM mode is determined by a resistance, input and output voltages, which are connected to the RT pin.



Forced PWM Mode



PFM Mode

● Enable Function

Standby state by inputting the "Low" to the EN pin, can be set to the active state by inputting the "High". When the EN pin voltage drops lower than 1.1 V, which is the EN "Low" input voltage (V_{ENL}), switching is turned off. When the EN pin voltage rises higher than 1.3 V, which is the EN "High" input voltage (V_{ENL}), the NC2780 starts and begins a soft start. The EN pin voltage must be 0.52V or less in order to make the current flowing through the VIN pin to the shutdown current (I_{SD}).
If enable function is not necessary, connect EN pin to VIN pin or other designated "High" voltage node at start-up.
Input voltage cannot be applied to the EN pin when no voltage is applied to the VIN pin.
However, please note that if the VIN pin and the EN pin are turned on at the same time with Ta > 125°C, it may occur the thermal shutdown detection state.

● MODE Switching Function

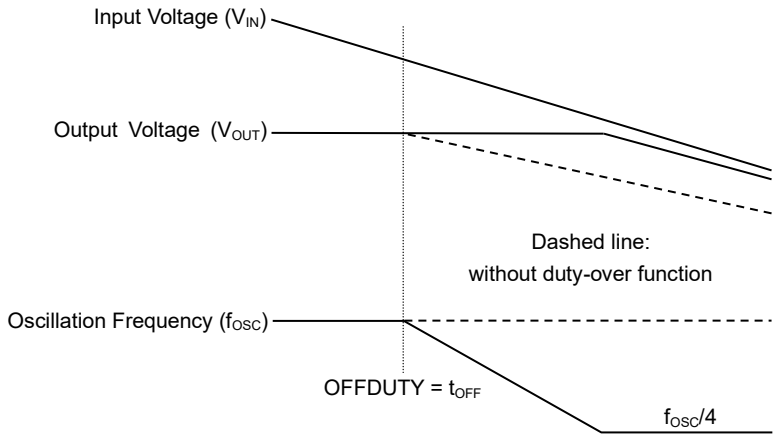
The NC2780 operating mode is switched among the forced PWM mode, PWM/PFM auto-switching mode and PLL_PWM mode, by a voltage or a pulse applied to MODE pin. The forced PWM mode is selected when the voltage of the MODE pin is more than 1.35 V, and the PWM works regardless of a load current. The PWM/PFM auto-switching mode is selected when it is less than 0.74 V, and control is switched between a PWM mode and a PFM mode depending on the load current. See Forced PWM mode and PFM mode for details. And see Frequency Synchronization Function for the operation on connecting an external clock.

● Frequency Synchronization Function

The NC2780 can synchronize to the external clock being inputted via the MODE pin, with using a PLL (Phase-locked loop). The forced PWM mode is selected during synchronization. The external clock with a pulse-width of 100 ns or more is required. The allowable range of oscillation frequency is 0.5 to 1.5 times of the set frequency(1), and the operating guaranteed frequency is in the 250 kHz to 1 MHz range(2). The NC2780 can synchronize to the external clock even if the soft-start works. That is, the NC2780 executes the soft-start and the synchronization functions at a time if having started up while inputting an external clock to the MODE pin.
When the maxduty or the duty-over state is caused by reduction in differential between input and output voltages, the device runs at asynchronous to the MODE pin, and it operates in the frequency reduced until one-fourth of the external clock frequency. Likewise, the CLKOUT pin becomes asynchronous to the MODE pin. If making synchronization to the MODE pin, take notice in use under a reduced input voltage.

● Duty-Over Function

When the input voltage is reduced at cranking, the operating frequency is reduced until one-fourth of the set frequency with being linearly proportional to time in order to maintain the output voltage. Exploiting the ON duty to exceed the maxduty value at normal operation can make the differential between input and output voltages small. The duty-over function enables when the minimum OFF time (t_{OFF}) is detected.

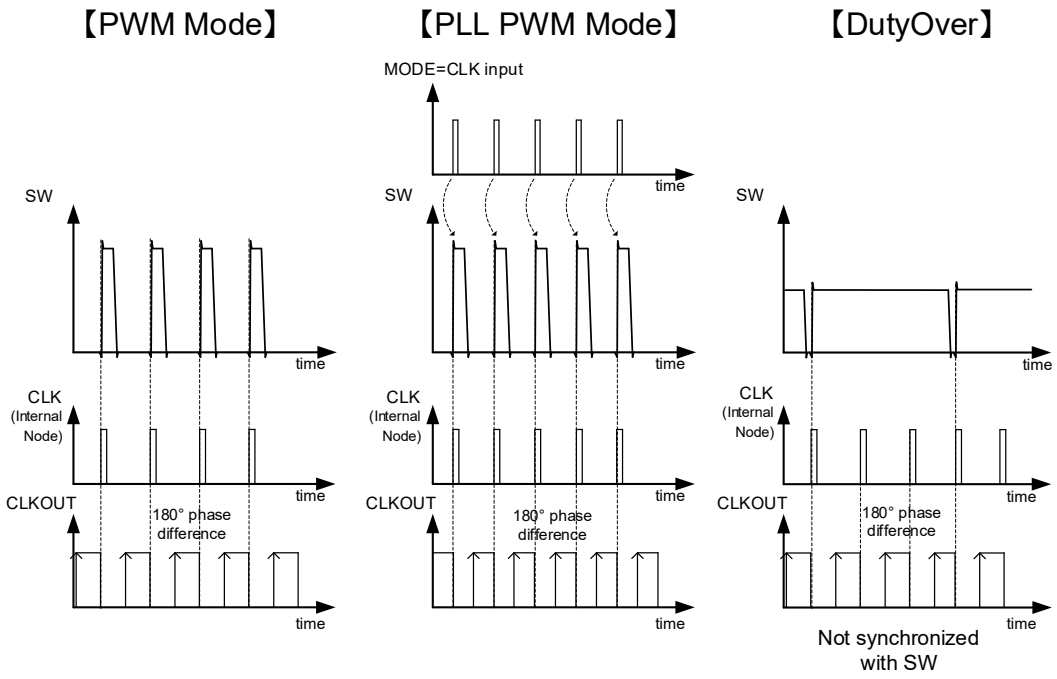


Frequency Modulation with Duty-Over

(1) See *Oscillation Frequency Setting* for details of the set frequency.
(2) The adjustable oscillation frequency range becomes 250kHz ≤ f_{OSC} ≤ 600kHz when 0.7 V ≤ V_{OUT} < 1.35V.

● CLKOUT Output Function

During PWM operation, the NC2780 outputs a pulse signal (Duty Typ. 50%) whose phase is 180° different from the switching control signal inside the IC from the CLKOUT pin. During PFM operation or BADFREQ detection, the CLKOUT pin is fixed in “Low”. It works for synchronized switching control signals, even during frequency synchronization.
Even in versions with the SSCG function enabled, the signal modulated by the SSCG is output along with the switching control signal. However, when the input voltage becomes close to the output voltage and the maximum duty or duty over state occurs, the operating frequency is controlled to be lowered relative to the switching control signals inside the IC, so the CLKOUT pin output becomes asynchronous with the operating frequency and does not match the frequency. If this function is not used, leave the CLKOUT pin open.



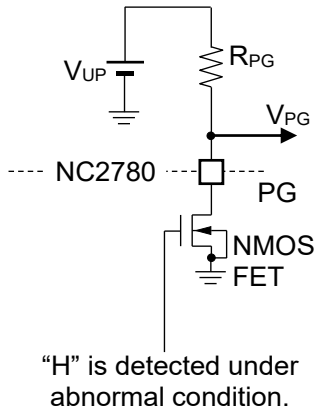
CLKOUT Output Image

● Power Good Output Function

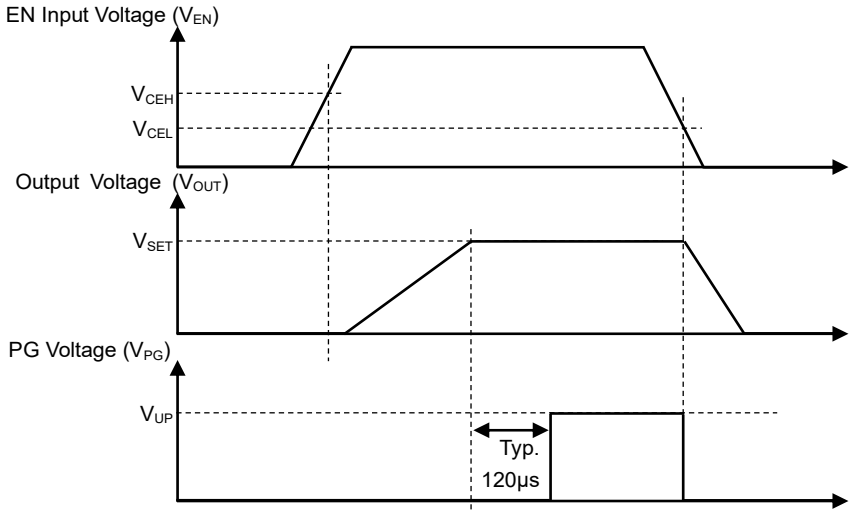
The power good function with using a NMOS open drain output pin can detect the following states of the NC2780. The NMOS FET turns on and the PG pin becomes "Low" when detecting them. When these conditions are released, the NMOS FET turns off and the PG pin outputs "High". (V_{UP} : PG pull-up Voltage).

・EN = "Low" (Shut Down)
・UVLO (Shut Down)
・Thermal Shut Down
・Soft-Start Time
・At UVD Threshold Voltage Detection
・At OVD Threshold Voltage Detection
・At Hiccup-Type Protection (when hiccup mode is selected)
・At Latch-Type Protection (when latch mode is selected)

The PG pin is designed to become 0.54 V or less in “Low” level when the current floating to the PG pin is 1 mA. The use of the PG pull-up voltage (V_{UP}) of 5.5 V or less and the pull-up resistor (R_{PG}) of 10 kΩ to 100 kΩ are recommended. If not using the PG pin, connect it to “Open” or “GND”.



Power Good Output Pin Connecting Diagram



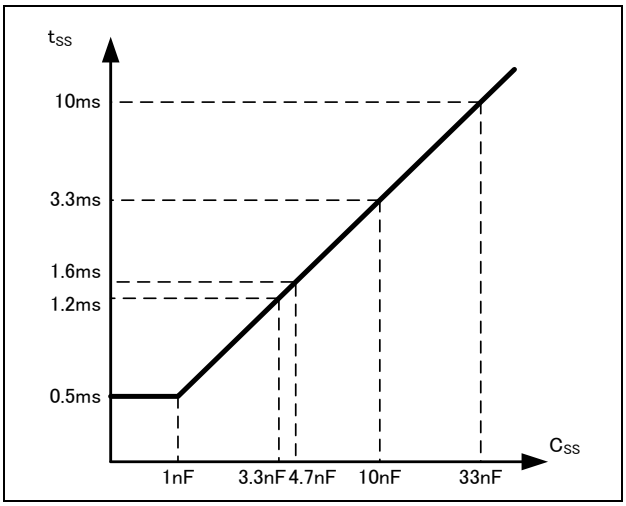
Rising / Falling Sequence of Power Good Circuit

● Soft-Start Function

The soft-start time is a time between a rising edge ("High" level) of the EN pin and the timing when the output voltage reaches the set output voltage. Connecting a capacitor (C_{SS}) to the CSS / TRK pin can adjust the soft-start time (t_{SS}) – provided the internal soft-start time of 500 µs (Typ.) as a lower limit. The adjustable soft-start time is 1.6 ms (Typ.) when connecting an external capacitor of 4.7 nF with the charging current of 2.0 µA (Typ.). If not required to adjust the soft-start time, set the CSS / TRK pin to “Open” to enable the internal soft-start time of 500 µs (Typ.). If connecting a large capacitor to an output signal, the overcurrent protection or the SW GND short protection might run. To avoid these protections caused by starting abruptly when reducing the amount of power current, soft-start time must be set as long as possible.

There is no upper limit on the capacitance value of C_{SS}.

Each of soft-start time (tss1/ tss2) is guaranteed under the conditions described in the chapter of “Electrical Characteristics”.

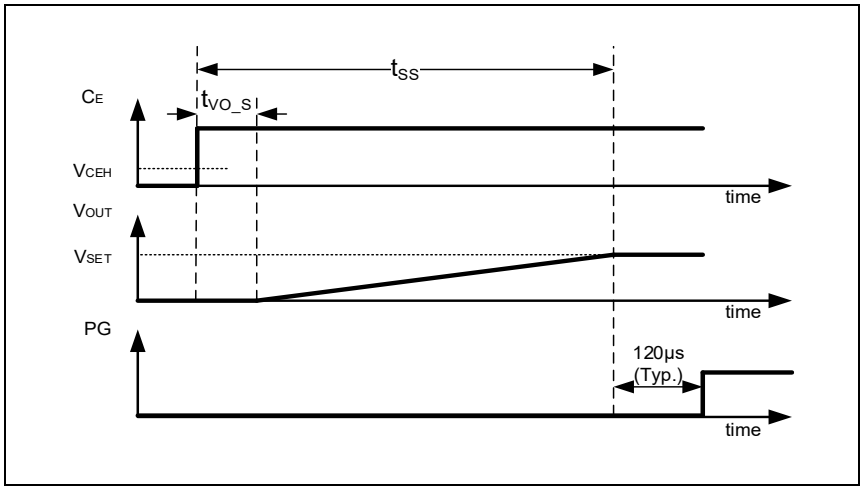


C_{SS} [nF] = (tss - t_{VO_S}) / 0.64 × 2.0

t_{SS}: Soft - Start time (ms)

t_{VO_S}: Time period from EN = “High” to VOUT’s rising (Typ. 0.160ms)

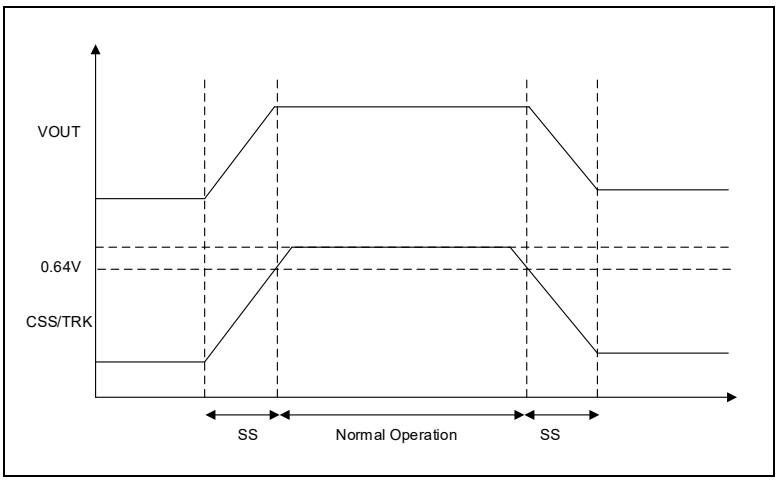
Soft-Start Time Adjustable Capacitor (C_{SS}) vs. Soft-Start Time (t_{SS})



Soft-Start Sequence

● Tracking Function

Applying an external tracking voltage to the CSS / TRK pin can control the soft-start sequence – provided that the lowest internal soft-start time is limited to 500 µs (Typ.). Since V_{FB} becomes nearly equal to $V_{CSS/TRK}$ at tracking, the complex start timing and soft-start can be easily designed. The available voltage at tracking is between 0 V and 0.64 V. If the tracking voltage is over 0.64 V, the internal reference voltage of 0.64 V is enabled. Also, an arbitrary falling waveform can be generated by reducing $V_{CSS/TRK}$ to 0.64 V (Typ.) or less, because the NC2780 supports both of up- and down- tracking.



Tracking Sequence

● Min. ON-Time

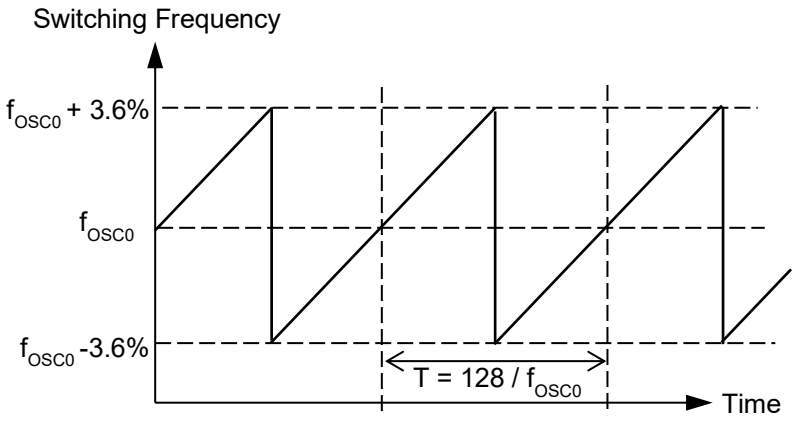
The min. ON time (Max.120 ns), which is determined in the NC2780 internal circuit, is a minimum time to turn high-side MOSFET on. The NC2780 cannot generate a pulse width less than the min. ON time. Therefore, settings of the output set voltage and the oscillator frequency are required so that the minimum step-down ratio [V_{OUT}/V_{IN} x (1 / f_{OSC})] does not stay below 120ns. If staying below 120 ns, the pulse skipping will operate to stabilize the output voltage. However, the ripple current and the output voltage ripple will be larger.

● Min. OFF-Time

By the adoption of bootstrap method, the high-side MOSFET, which is used as the NC2780 internal circuit for the min. OFF time, is used a NMOS. The voltage sufficient to drive the high-side MOSFET must be charged. Therefore, the min. OFF time is determined from the required time to charge the voltage. By the adoption of the frequency's reduction method by one-quarter of a set value (Min.), if the input-output difference voltage becomes small or load transients are caused, the OFF period can be caused once in four-cycle period of normal cycle. As a result, the min. OFF time becomes 190 ns (Typ.) substantially, and the maximum duty cycle can be improved.
When the input voltage is low or there is a sudden load transient, the duty over function turns off the high-side MOSFET every four cycles at the minimum, effectively increasing the maximum duty ratio to reduce the input-output voltage difference.

● **SSCG (Spread Spectrum Clock Generator)**

In order to reduce the interference of conductive / radioactive noise, we have prepared an option of SSCG (Spread Spectrum Clock Generator) function. SSCG function is valid during PWM operation. SSCG suppresses the peak noise by spreading the switching frequency in a specific range. In this version, the switching frequency (f_{OSC}) changes with the ramp wave within a range of ± 3.6% (Typ.) of set frequency. The modulation cycle is 128 / f_{OSC}. See the figure below. SSCG is valid only during PWM operation and disabled during PFM operation. Also note that the SSCG is invalid when an external clock is applied. Note that the effect of SSCG cannot be obtained when an external clock is input. Also, modulation of ramp wave cannot be maintained during pulse-skipping operation to prevent overvoltage.



Fluctuation Diagram of Oscillation Frequency by SSCG

PROTECTION FUNCTION

● Thermal Shutdown

When the junction temperature exceeds the thermal shutdown detection temperature (Typ.160°C), switching stops and self-heating is suppressed.
This IC will restart when the junction temperature drops below the thermal shutdown release temperature (Typ.140°C). Then, the Soft-Start function is activated.

● SW Power Supply (VIN Short) / GND (GND Short) Protection

In addition to normal current limit, the NC2780 provides the SW power supply / GND short protection to monitor the voltage between the MOSFET's drain and source. Since the current limit function is controlled with an external inductor's DCR or a sense resistance, the current limit function cannot work when a through-current is flowed through the MOSFET and when an overcurrent is generated by shorting the SW pin to VDD/GND. The detecting current is determined by SW shot to VDD/GND detector threshold voltage (ON-resistance of MOSFET x Current, Typ.0.43 V).

● Current Limit Function

The current limit function can be to limit the current by the peak current method to turn the high-side MOSFET off that the potential differences is over the current limit threshold voltage. The threshold voltage is selectable among 50 mV / 70 mV / 100 mV.
The current limit value is detected with the voltage across a sense resistance that is connected to the inductor in series. By connecting a resistance with low level of variation, the current limit with high accuracy can achieve.
As a result, be caution that the power loss is caused from the current and R_{SENSE}. The peak current in the current limit inductor can be calculated by the following equation.

Peak Current in Current Limit Inductor (A) = Current Limit Threshold Voltage (mV) / R_{SENSE} (mΩ)

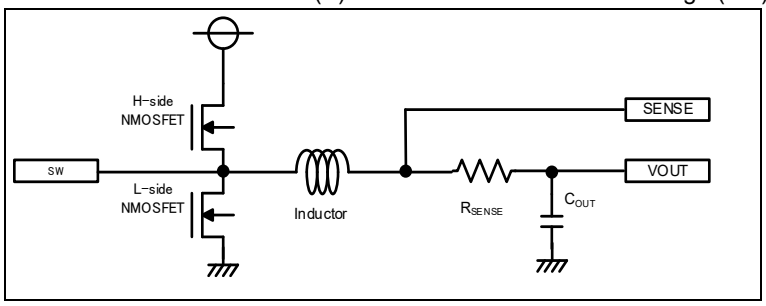


Figure A Detection with Sense Resistance

Even if a sense resistor is not connected, it is possible to control the current limit value using the DCR of an inductor, but this is not recommended as that the accuracy will deteriorate significantly.

● Reverse Current Limit Function

The reverse current limit function can be to limit the current by the peak current method to turn the low-side MOSFET off that the potential differences between voltage of VOUT and SENSE is below the reverse current limit threshold voltage.
Reverse current limit inductor peak current is calculated by the following equation.

Reverse current limit inductor peak current (A) = Reverse Current Limit Threshold Voltage (mV) / R_{SENSE} (mΩ)

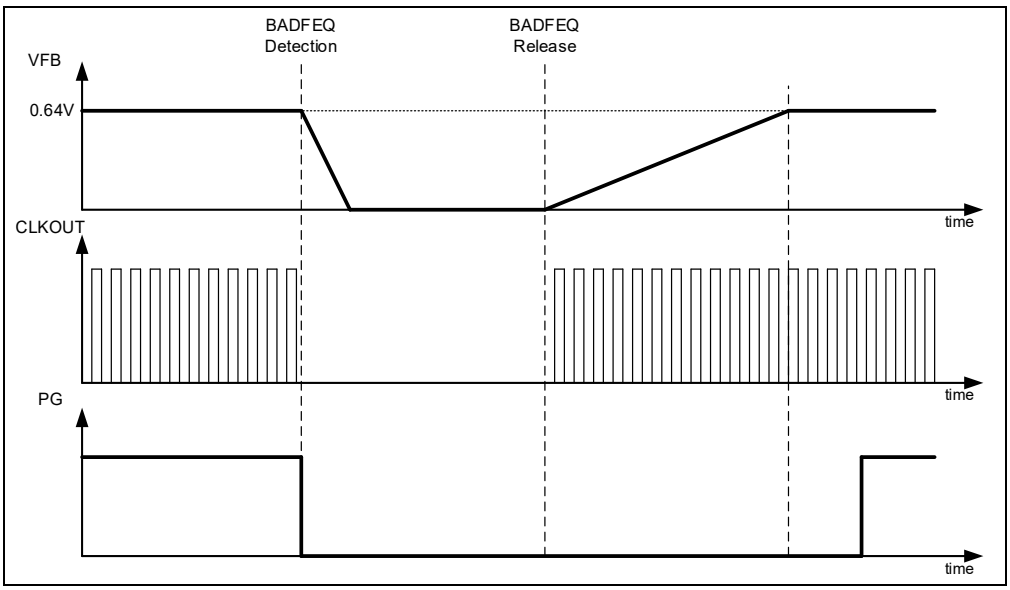
This function mainly operates when the output is tied to a voltage higher than the set output voltage in some reasons.

● Through-Current Protection

The HGATE pin voltage (V_{HGATE}) and the LGATE pin voltage (V_{LGATE}) are monitored to protect a through-current caused by an external MOSFET. In the case of turning-on the low-side MOSFET, after a difference between V_{HGATE} - SW pin voltage (V_{SW}) becomes 1V or less, increasing V_{LGATE} can prevent not to turn on both of the high-side and low-side MOSFETs at a time and thereby prevent the through-current. In the case of turning-on the high-side MOSFET, after a difference between V_{LGATE} - GND (PGND pin voltage) becomes 1 V or less, increasing a difference between V_{HGATE} - V_{SW} can prevent the through-current.

● Bad Frequency (BADFREQ) Protection

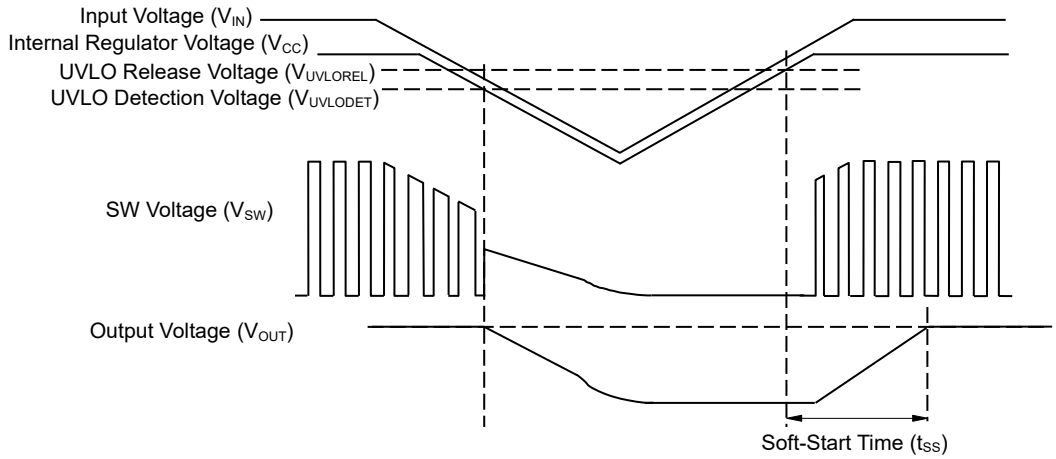
If a current equivalent to 2 MHz (Typ.) or more or 125 kHz (Typ.) or less is applied to the RT pin when the resistor of the RT pin is in open / short, the NC2780 will stop switching to protect the IC and will cause the internal state to transition to its state before the soft-start. The CLKOUT pin is fixed to "Low" while the bad frequency as above is detected. The NC2780 will restart under the normal control from the state of soft-start when recover after the abnormal condition.



BADFREQ Detection / Release Sequence

● UVLO (Undervoltage Lockout) Function

The UVLO function is a function that prevents malfunction by turning off switching when the VCC pin voltage becomes lower than the UVLO detection voltage ($V_{UVLODET}$) due to a drop in the input voltage. Since switching stops, the output voltage drops depending on the load and C_{OUT}. When the VCC pin voltage rises above the UVLO release voltage ($V_{UVLOREL}$), the NC2780 restarts and begins a soft start.



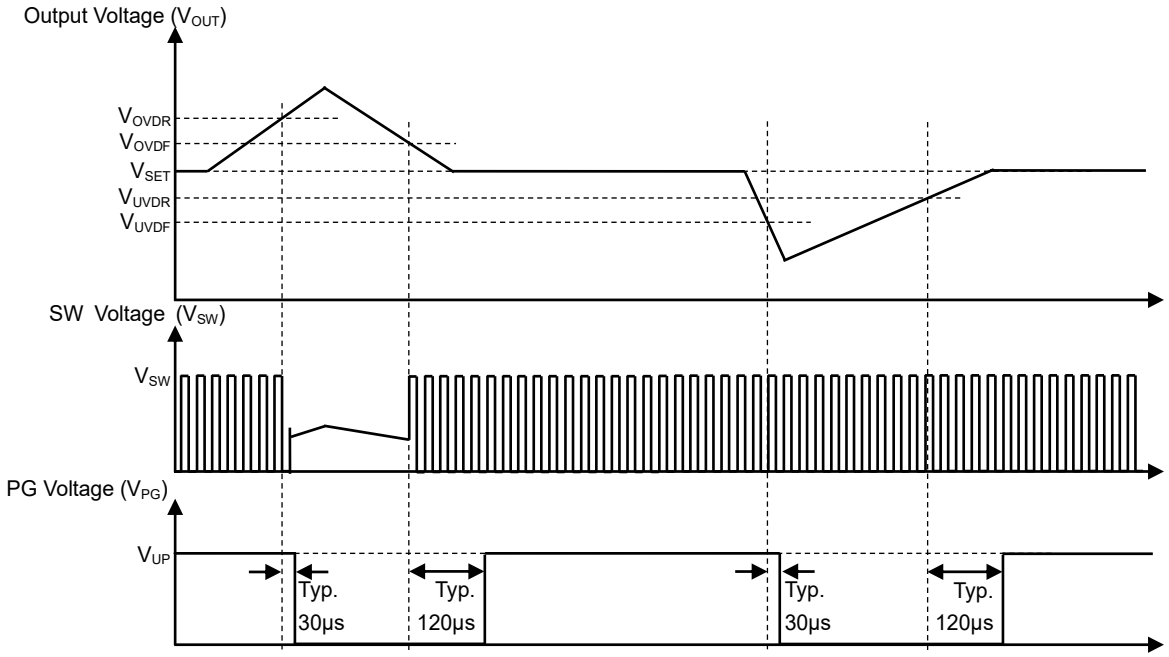
UVLO Timing Chart

● Under Voltage Detection (UVD)

The UVD function indirectly monitors the output voltage with using the FB pin. The PG pin outputs "Low" when the UVD detector threshold is 90% (Typ.) of V_{FB} and V_{FB} is less than the UVD detector threshold for more than 30 µs (Typ.). When V_{FB} is over 93% (Typ.) of 0.64 V, the PG pin outputs "High" after delay time (Typ.120 µs). And, the hiccup- / latch-type overcurrent protection works when detecting an overcurrent, an SW power supply protection, or an over voltage protection during the UVD detection.

● Over Voltage Detection (OVD)

The OVD function indirectly monitors the output voltage with using the FB pin. Switching stops even if the internal circuit is active state, when detecting the over voltage of V_{FB}. The PG pin outputs "Low" when the OVD detector threshold is 110% (Typ.) of V_{FB} and V_{FB} is over the OVD detector threshold for more than 30 µs (Typ.). When V_{FB} is under 107% (Typ.) of V_{FB}, which is the OVD released voltage, the PG pin outputs "High" after delay time (Typ.120 µs). Then, switching is controlled by normal operation. The over voltage protection works when an error is caused by a feedback resistor in peripheral circuits for the FB pin.



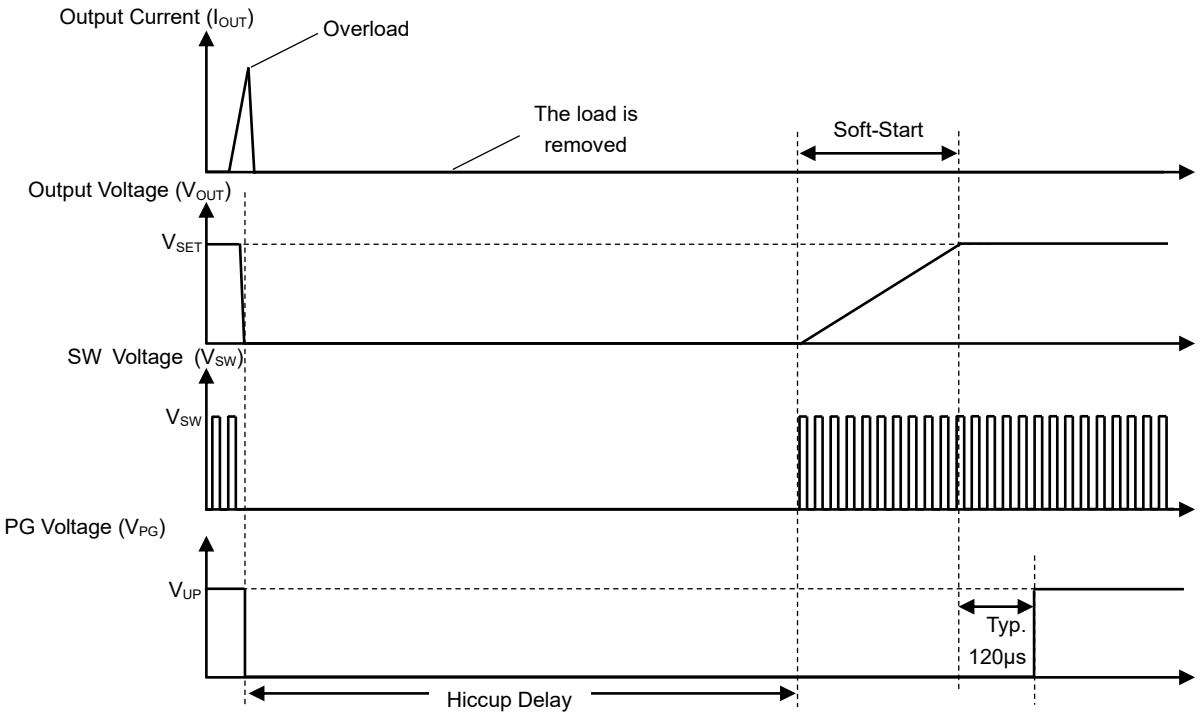
Over Voltage Detection / Under Voltage Detection Sequence

● Over Voltage Protection (OVP)

The OVP function monitors the voltage of VOUT pin to reduce an over voltage, when an error is caused in peripheral circuits for the FB pin. Switching stops even if the internal circuit is active state, when V_{OUT} is over the OVP detector threshold. When V_{OUT} is under the OVP detector threshold, switching is controlled by normal operation. If the UVD for FB pin occur during the OVP detect state, an error will occur and hiccup- / latch-type protection will work. However, the operation under this function is not guaranteed because the OVP detector threshold is set to the absolute maximum rating and more for the VOUT pin.

● Hiccup-Type / Latch-Type Overcurrent Protection

The hiccup-type / latch-type overcurrent protection can work under the operating conditions that is the UVD can function during the current limit or OVP and the SW GND short protection. The latch-type protection can release the circuit by setting the EN pin to "Low" or by reducing V_{IN} to be less than the UVLO detector threshold, when the output is latched off. The hiccup type protection stops switching releases the circuit after the protection delay time (Typ. 3.5 ms). Since this protection is auto-release, the EN pin switching of "Low" / "High" is unnecessary. And damage due to the overheating might not be caused because the term to release is long. When the output is shorted to GND, switching of "ON" / "OFF" is repeated until the short circuit condition is released.



Timing Chart of Hiccup Type Overcurrent Protection

THERMAL CHARACTERISTICS (HSOP-18-AK)

Thermal characteristics depend on mounting conditions. The thermal characteristics below are the results of measurements under measurement conditions determined by our company with reference to JEDEC STD. (JESD51).

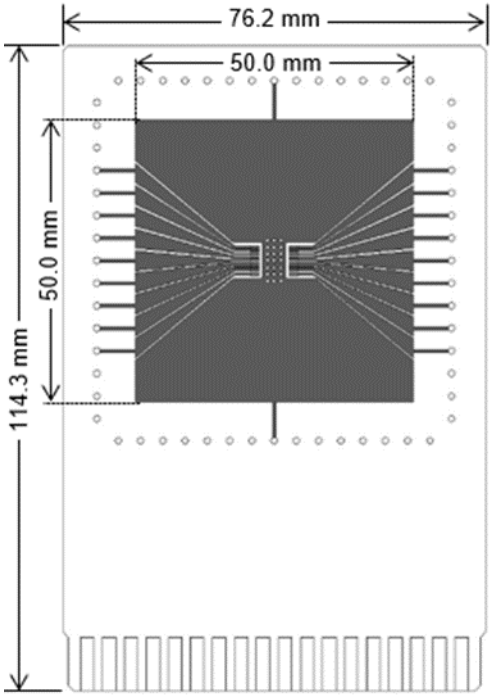
Measurement Result

Item	Measurement Result
Thermal Resistance (θja)	32 °C/W
Thermal Characterization Parameter (ψjt)	8 °C/W

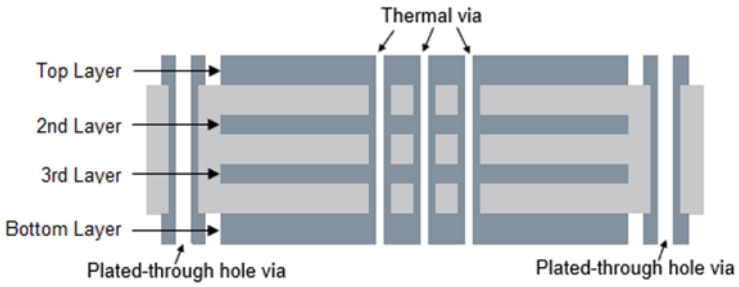
θja : Junction-to-Ambient Thermal Resistance
ψjt : Junction-to-Top Thermal Characterization Parameter

Measurement Conditions

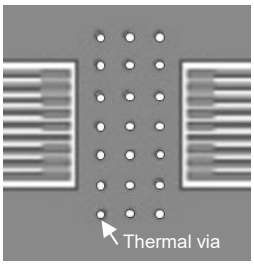
Item		Specification
Measurement Condition		Mounting on Board (Still Air)
Board material		FR-4
Board size		76.2 mm × 114.3 mm × t 0.8 mm
Copper foil layer	1	50 mm × 50 mm (coverage rate 95%), t 0.040 mm
	2	50 mm × 50 mm (coverage rate 100%), t 0.035 mm
	3	50 mm × 50 mm (coverage rate 100%), t 0.035 mm
	4	50 mm × 50 mm (coverage rate 100%), t 0.040 mm
Thermal vias		ϕ 0.3 mm × 21 pcs



Measurement Board Pattern



Cross section view of layers and vias



Enlarged view of IC mounting area

CALCULATION METHOD OF JUNCTION TEMPERATURE

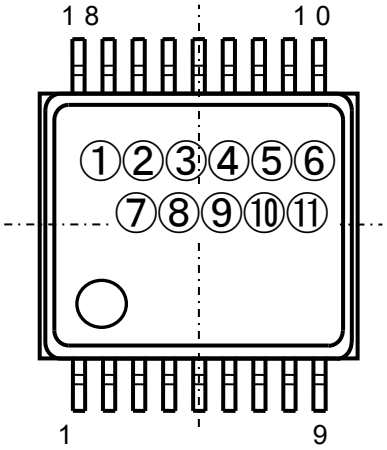
The junction temperature (Tj) can be calculated from the following equation.

$T_j = T_a + \theta ja \times P$
$T_j = Tc\ (top) + \psi jt \times P$

T_a : Ambient temperature
Tc (top) : Package mark side center temperature
P : Power consumption under user's conditions

MARKING SPECIFICATION

①②③④⑤⑥⑦⑧⑨ : Product Code ⋯ **Refer to the following table**
⑩⑪ : Lot Number ⋯ Alphanumeric Serial Number



HSOP-18-AK Marking Specification

NOTICE

There can be variation in the marking when different AOI (Automated Optical Inspection) equipment is used. In the case of recognizing the marking characteristic with AOI, please contact our sales or distributor before attempting to use AOI.

NC2780 Marking List

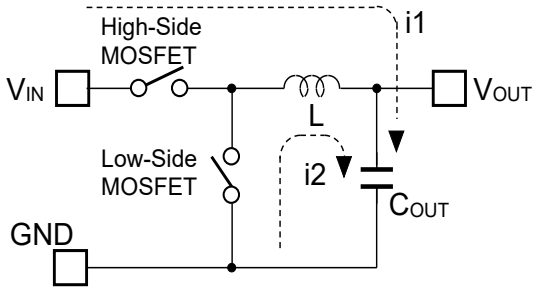
Product Name	①②③④⑤⑥⑦⑧⑨
NC2780AK001AE2D	C 2 7 8 0 A 0 0 1
NC2780AK001BE2D	C 2 7 8 0 B 0 0 1
NC2780AK001CE2D	C 2 7 8 0 C 0 0 1
NC2780AK001DE2D	C 2 7 8 0 D 0 0 1
NC2780AK002AE2D	C 2 7 8 0 A 0 0 2
NC2780AK002BE2D	C 2 7 8 0 B 0 0 2
NC2780AK002CE2D	C 2 7 8 0 C 0 0 2
NC2780AK002DE2D	C 2 7 8 0 D 0 0 2
NC2780AK003AE2D	C 2 7 8 0 A 0 0 3
NC2780AK003BE2D	C 2 7 8 0 B 0 0 3
NC2780AK003CE2D	C 2 7 8 0 C 0 0 3
NC2780AK003DE2D	C 2 7 8 0 D 0 0 3

Product Name	①②③④⑤⑥⑦⑧⑨
NC2780AK101AE2D	C 2 7 8 0 A 1 0 1
NC2780AK101BE2D	C 2 7 8 0 B 1 0 1
NC2780AK101CE2D	C 2 7 8 0 C 1 0 1
NC2780AK101DE2D	C 2 7 8 0 D 1 0 1
NC2780AK102AE2D	C 2 7 8 0 A 1 0 2
NC2780AK102BE2D	C 2 7 8 0 B 1 0 2
NC2780AK102CE2D	C 2 7 8 0 C 1 0 2
NC2780AK102DE2D	C 2 7 8 0 D 1 0 2
NC2780AK103AE2D	C 2 7 8 0 A 1 0 3
NC2780AK103BE2D	C 2 7 8 0 B 1 0 3
NC2780AK103CE2D	C 2 7 8 0 C 1 0 3
NC2780AK103DE2D	C 2 7 8 0 D 1 0 3

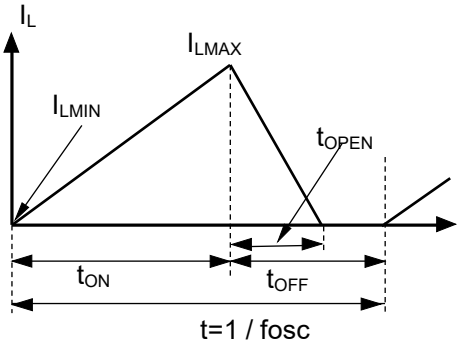
APPLICATION NOTE

● Operation of Step-Down Switching Regulator

A basic step-down switching regulator is illustrated in the following figures. This switching regulator charges energy in the inductor when the high-side MOSFET turns on, and discharges the energy from the inductor when the high-side MOSFET turns off and controls with less energy loss, so that a lower output voltage than the input voltage is obtained.



Basic Circuit



Current Through Inductor

Step1. The high-side MOSFET turns on and current IL (= i1) flows, and energy is charged into C_{OUT}. At this moment, I_L increases from I_{LMIN} (= 0) to reach I_{LMAX} in proportion to the On-time period (ton) of the high-side MOSFET turns on and current I_L (= i1) flows, and energy is charged into C_{OUT}. At this moment, I_L increases from I_{LMIN} (= 0) to reach I_{LMAX} in proportion to the On-time period (t_{ON}) of the high-side MOSFET.

Step2. When the high-side MOSFET turns off, the low-side MOSFET turns on in order to maintain I_L at I_{LMAX}, and current I_L (= i2) flows.

Step3. **When MODE = Low (PFM / PWM Auto-Switching Mode),**
I_L (= i2) decreases gradually and reaches $I_L = I_{LMIN} = 0$ after a time period of t_{OPEN}, and the low-side MOSFET turns off. This case is called as discontinuous mode. The PFM mode is switched if go to the discontinuous mode. If the output current is increased, a time period of t_{OFF} runs out prior to reach of $I_L = I_{LMIN} = 0$. The result is that the high-side MOSFET turns on and the low-side MOSFET turns off in the next cycle. This case is called continuous mode. Upon entering this continuous mode, NC2780 will transition to the PWM mode.
When MODE = High (Forced PWM Mode), MODE = External Clock (PLL_PWM Mode),
Since the continuous mode works at all time, the low-side MOSFET turns on until going to the next cycle. That is, the low-side MOSFET must keep "On" to meet $I_L = I_{LMIN} < 0$, when reaches $I_L = I_{LMIN} = 0$ after a time period of t_{OPEN}.

In the PWM mode, the output voltage is maintained constant by controlling t_{ON} with the constant switching frequency (f_{OSC}).
In PFM mode, t_{ON} is constant and the output voltage is kept constant by controlling f_{OSC}.

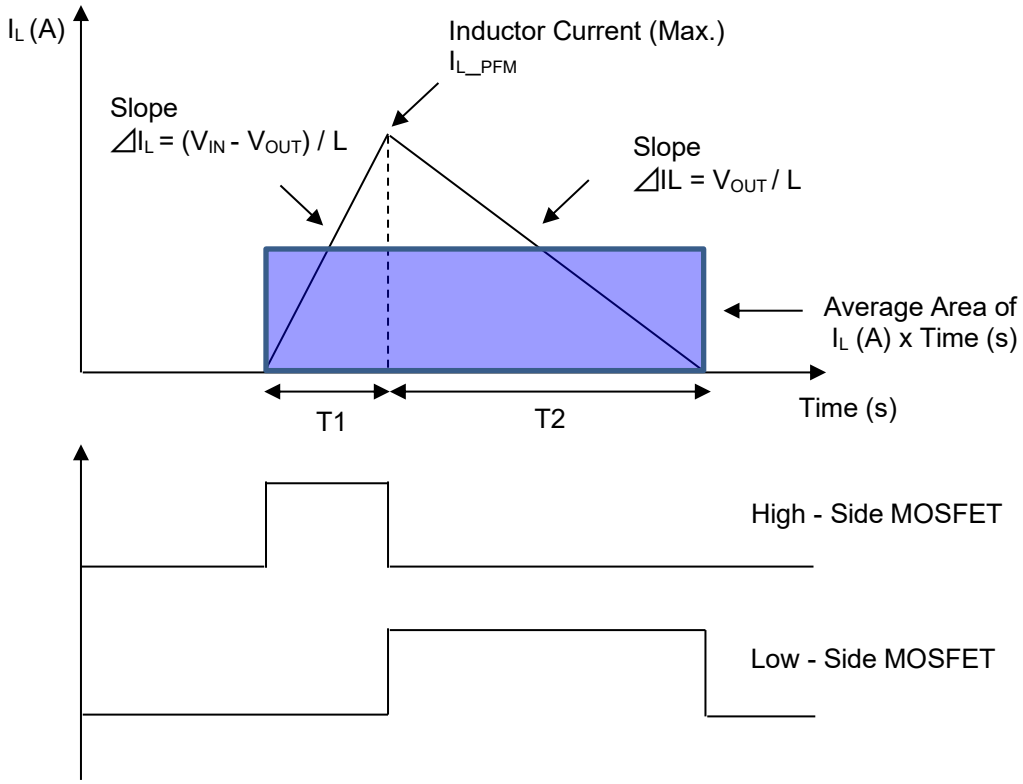
● Calculation of PFM Ripple

Calculation example of output ripple voltage (V_{OUT_PFM}) is described. V_{OUT_PFM} can be calculated by Equation 1. And, the maximum value of inductor current (I_{L_PFM}) can be calculated by Equation 2.

$$V_{OUT_PFM} = R_{COUT_ESR} \times (I_{L_PFM}) + C_{OEF_TON_PFM} \times (I_{L_PFM} / 2) / f_{OSC} / C_{OUT_EFF} \quad \cdots\cdots \text{Equation 1}$$

$$I_{L_PFM} = ((V_{IN} - V_{OUT}) / L) \times C_{OEF_TON_PFM} \times V_{OUT} / V_{IN} / f_{OSC} \quad \cdots\cdots \text{Equation 2}$$

V_{OUT_PFM} : Output ripple
R_{COUT_ESR} : ESR of output capacitor
I_{L_PFM} : Maximum current of inductor
$C_{OEF_TON_PFM}$: Scaling factor of On-time - Typ.1.54X (Design value)
$(V_{IN} - V_{OUT}) / L$: Slope of inductor current
$C_{OEF_TON_PFM} \times V_{OUT} / V_{IN} / f_{OSC}$: On-time



Inductor Current Waveform at PFM Mode

Output voltage can be calculated by the following simple equation.

$V_{OUT} = I \times T / C$
I : Current, C : Capacitance, T : Time

Since I is represented by "1/2 x I_{L_PFM}" as the average current, the time of current passing at the PFM mode can be expressed by the following equation.

$T = C_{OEF_TON_PFM} / f_{OSC}$

And, the output ripple voltage (V_{OUT_PFM}) is superimposed a voltage for ESR × I, and Equation 1 is determined. But, ESR is so small that it may be ignored if ceramic capacitors are connected in parallel.

The amount of charge to the output capacitor can be calculated by Equation 3.

(High-side MOSFET On-time (T1) + Low-side MOSFET On-time (T2)) × Average amount of current ···· Equation 3

Then, T1 and T2 can be calculated by the following equations, and the time of current passing can be determined.

$T1 = C_{OEF_TON_PFM} / f_{OSC} \times V_{OUT} / V_{IN}$ ····· (On-time at PFM)
$T2 = (V_{IN} / V_{OUT}\text{-}1) \times T1$ ($0 = I_{L_PFM} - V_{OUT} / L \times T2$)

$T = T1 + T2$
$= V_{IN} / V_{OUT} \times T1$
$= C_{OEF_TON_PFM} / f_{OSC}$

And then, the amount of charge can be determined as Equation 4.

$T \times I_{L_PFM} / 2 = {}_{OEF_TON_PFM} / f_{OSC} \times I_{L_PFM} / 2$ ····· Equation 4

With using above equations, the output ripple voltage (V_{OUT_PFM}) can be calculated by Equation 5.

$V = IT / C = C_{OEF_TON_PFM} / f_{OSC} \times I_{L_PFM} / 2 / C_{OUT_EFF}$ ····· Equation 5

● Output Voltage Setting

The output voltage (V_{OUT}) can be set by adjustable values of R_{TOP} and R_{BOT}. The value of V_{OUT} can be calculated by Equation1.

$$V_{OUT} = V_{FB} \times (R_{TOP} + R_{BOT}) / R_{BOT} \quad \cdots\cdots \text{Equation 1}$$

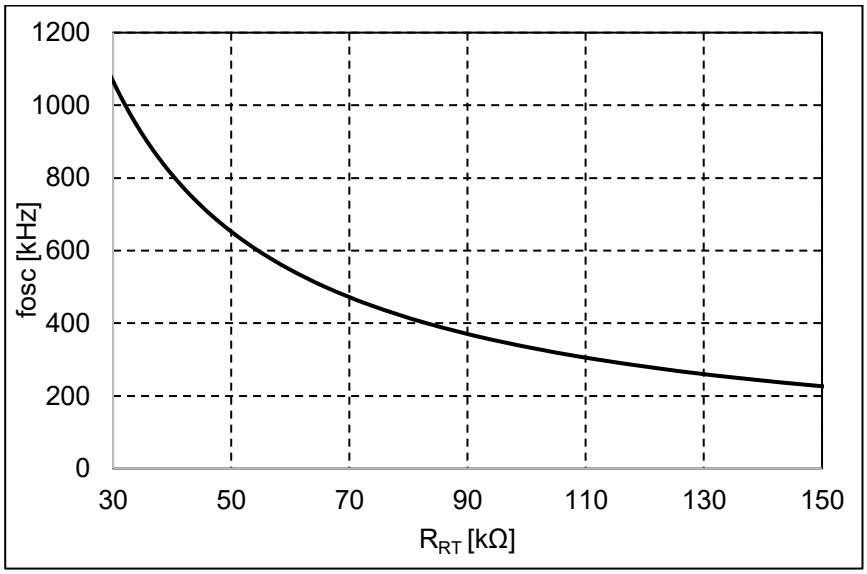
For example, when setting V_{OUT} = 3.3 V and setting R_{BOT} = 22 kΩ, R_{TOP} can be calculated by substituting them to Equation 1. As a result of the expanding Equation 2, R_{TOP} can be set to 91.4 kΩ.
To make 91.4 kΩ with using the E24 type resistors, the connecting use of 91 kΩ and 0.39 kΩ resistors in series is required. If the tolerance level of the set output voltage is wide, using a resistor of 91 kΩ to R_{TOP} can reduce the number of components.

$$R_{TOP} = (3.3V / 0.64V - 1) \times 22k\Omega$$
$$= 91.4k\Omega \quad \cdots\cdots \text{Equation 2}$$

As to NC2780AK001x, NC2780AK002x, NC2780AK003x, R_{TOP} and R_{BOT} should be selected to meet the required output voltage (V_{OUT}) > 2.91 V with a variation in resistance taken into account.

● Oscillation Frequency Setting

Connecting the oscillation frequency setting resistor (R_{RT}) between the RT pin and GND can control the oscillation frequency in the range of 250 kHz to 1 MHz[3]. For example, using the resistor of 66 kΩ can set the frequency of about 500 kHz.
The Electrical Characteristics guarantees the oscillation frequency under the conditions stated below for f_{OSC0} (at R_{RT} = 135 kΩ) and f_{OSC1} (at R_{RT} = 32 kΩ).

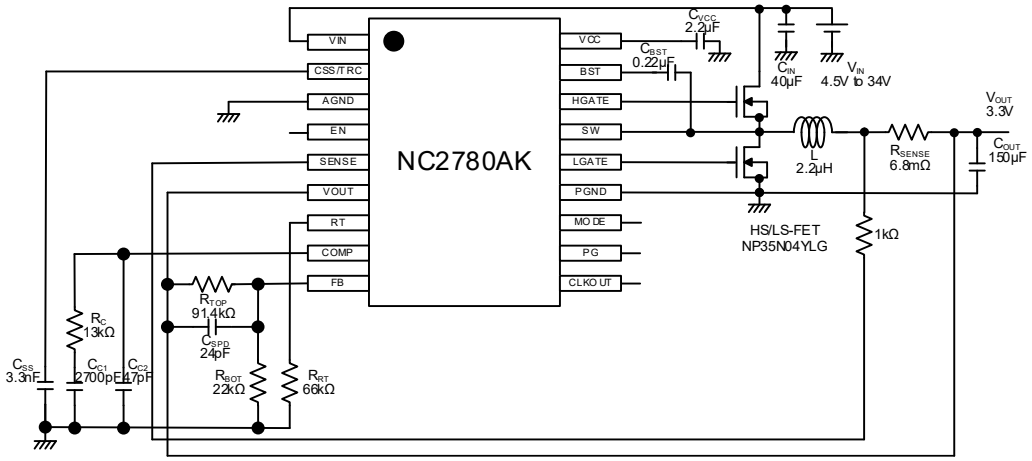


R_{RT} [kΩ] = 41993 × fosc [kHz] ^ (-1.039)
Oscillation Frequency Setting Resistor (R_{RT}) vs. Oscillation Frequency (f_{OSC})

[3] The adjustable oscillation frequency range becomes 250 kHz ≤ f_{OSC} ≤ 600 kHz when 0.7 V ≤ V_{OUT} < 1.35V.

● Selection of External Components

External components and its value required for NC2780 are described. Each value is reference value at initial.
Since inductor's variations and output capacitor's effective value may lead a drift of phase characteristics, adjustment to a unity-gain and phase characteristics may be required by evaluation on the actual unit.



NC2780AK Typical Application Circuit

1. Determination of Requirements

Determine the frequency, the output capacitor, and the input voltage required. For reference values, parameters listed in the following table will be used to explain each equation.

Output Voltage (V_{OUT}) : 3.3V
Output Current (I_{OUT}) : 10A
Input Voltage (V_{IN}) : 12V
Input Voltage Range : 8V to 16V
Frequency (f_{OSC}) : 500kHz
ESR of Output Capacitor ESR (R_{COUT_ESR}) : 3mΩ

2. Selection of Unity-gain Frequency (f_{UNITY})

The unity-gain frequency (f_{UNITY}) is determined by the frequency that the loop gain becomes "1" (zero dB). It is recommended to select within the range of one-sixth to one-tenth of the oscillator frequency (f_{OSC}). Since the f_{UNITY} determines the transient response, the higher the f_{UNITY}, the faster response is achieved, but the phase margin will be tight. Therefore, it is required that the f_{UNITY} can secure the adequate stability. As for the reference, the f_{UNITY} is set to 70 kHz.

3. Selection of Inductor

After the input and the output voltages are determined, a ripple current (ΔI_L) for the inductor current is determined by an inductance (L) and an oscillator frequency (f_{OSC}). The ripple current (ΔI_L) can be calculated by Equation 1.

$$\Delta I_L = (V_{OUT} / L / f_{OSC}) \times (1 - V_{OUT} / V_{IN_MAX}) \cdots\cdots \text{Equation 1}$$

V_{IN_MAX}: Maximum input voltage

The core loss in the inductor and the ripple current of the output voltage become small when the ripple current (ΔI_L) is small. But, a large inductance is required as shown by Equation 1. The inductance can be calculated by Equation 2 when a reference value of ΔI_L assumes 30% of I_{OUT} is appropriate value.

$$L = (V_{OUT} / \Delta I_L / f_{OSC}) \times (1 - V_{OUT} / V_{IN_MAX}) \cdots\cdots \text{Equation 2}$$
$$= (V_{OUT} / (I_{OUT} \times 0.3) / f_{OSC}) \times (1 - V_{OUT} / V_{IN_MAX})$$

The inductance can be calculated by substituting each parameter to Equation 2.

$$L = (3.3V / 10A \times 0.3 / 500kHz) \times (1 - 3.3V / 16V) = 1.75\mu H$$

When selecting the inductor of 2.2µH as an approximate value of the above calculated value, ΔI_L can be shown as below.

$$\Delta I_L = (3.3V / 2.2\mu H / 500kHz) \times (1 - 3.3V / 16V) = 2.38A$$

4. Setting of Output Capacitance

The output capacitance (C_{OUT}) must be set to meet the following conditions.

4-1. Calculation based on phase margin

To secure the adequate stability, it is recommended that the pole frequency (f_{P_OUT}) is set to become equal or below one-fourteenth of the unity-gain frequency. The pole frequency (f_{P_OUT}) can be calculated by Equation 3.

$$f_{P_OUT} = 1 / (2 \times \pi \times C_{OUT_EFF} \times ((R_{OUT_MIN} \times 2 \times \pi \times f_{OSC} \times L) / (R_{OUT_MIN} + 2 \times \pi \times f_{OSC} \times L) + R_{COUT_ESR})) \quad \cdots\cdots \text{Equation 3}$$

C_{OUT_EFF}: Output capacitance (effective value)
R_{OUT_MIN}: Output resistance at maximum output current
$R_{OUT_MIN} = V_{OUT} / I_{OUT}$
$= 3.3V / 10A$
$= 0.33\Omega$

Equation (4) can be expressed by substituting $f_{P_OUT} = f_{UNITY} / 14$ to Equation 3.

$$C_{OUT_EFF} = 14 / (2 \times \pi \times \mathbf{f_{UNITY}} \times ((R_{OUT_MIN} \times 2 \times \pi \times f_{OSC} \times L) / (R_{OUT_MIN} + 2 \times \pi \times f_{OSC} \times L) + R_{COUT_ESR})) \quad \cdots\cdots \text{Equation 4}$$

Then, the output capacitance (effective value) can be calculated by substituting each parameter to Equation 4

$$C_{OUT_EFF} = 14 / (2 \times \pi \times 70kHz \times ((0.33\Omega \times 2 \times \pi \times 500kHz \times 2.2\mu H) / (0.33\Omega + 2 \times \pi \times 500kHz \times 2.2\mu H) + 3m\Omega))$$
$$= 100.1\mu F$$

It is recommended that the output capacitance is set to become equal or over the effective value calculated by Equation 4

The effective value of capacitor capacitance varies with the applied DC voltage. Equation 5 below shows calculation formula for ceramic capacitors. Please refer to capacitor specification for more accurate bias characteristics.

$$C_{OUT_EFF} = C_{OUT_SET} \times (V_{CO_AB} - V_{OUT}) / V_{CO_AB} \quad \cdots\cdots \text{Equation 5}$$

C_{OUT_SET}: Output capacitor's spec
V_{CO_AB}: Capacitor's voltage rating

With using Equation 5, the effective value is calculated to become 100.1 µF or more. The output voltage (C_{OUT}) can be shown as below when V_{CO_AB} is 10 V.

$C_{OUT_SET} > C_{OUT_EFF} / ((V_{CO_AB} - V_{OUT}) / V_{CO_AB})$
$C_{OUT_SET} > 100.1\mu F / ((10 - 3.3) / 10)$
$C_{OUT} > 149.4\mu F$

As the calculated result, C_{OUT} selects a capacitor of 150 µF (the effective value is 100.5 µF)

4-2. Calculation based on ripple at PFM mode.
With using the calculated value of C_{OUT}, the amount of ripple at the PFM mode can be shown as Equation 6 and Equation 7.

$$I_{L_PFM} = ((V_{IN_MAX} - V_{OUT}) / L) \times C_{OEF_TON_PFM} \times V_{OUT} / V_{IN_MAX} / f_{OSC} \cdots\cdots \text{Equation 6}$$
$$V_{OUT_PFM} = R_{COUT_ESR} \times (I_{L_PFM}) + C_{OEF_TON_PFM} \times (I_{L_PFM} / 2) / f_{OSC} / C_{OUT_EFF} \cdots\cdots \text{Equation 7}$$

I_{L_PFM}: Maximum inductor current
$C_{OEF_TON_PFM}$: On-time scaling (multiples of PFM_On time)
V_{OUT_PFM}: Maximum output ripple

$C_{OEF_TON_PFM}$ can be calculated by 1.54 times (Typ.) as the design value. The ripple value can be calculated by substituting each parameter to Equation 6 and Equation 7.

$$I_{L_PFM} = ((16V - 3.3V) / 2.2\mu H) \times 1.54 \times 3.3V / 16V / 500kHz$$
$$= 3.67\ A$$
$$V_{OUT_PFM} = 3m\Omega \times 3.67A + 1.54 \times (3.67A / 2) / 500kHz / 100.5\mu F$$
$$= 67.2mV$$

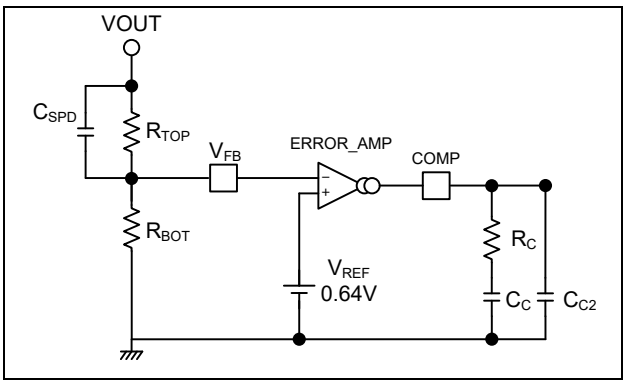
V_{OUT_PFM} must be set to become the target ripple value or less. If V_{OUT_PFM} is over the target value, the output capacitance must be calculated by Equation 8.

$$C_{OUT_EFF} = 1.54 \times (I_{L_PFM} / 2) / f_{OSC} / (V_{OUT_PFM} - R_{COUT_ESR} \times (I_{L_PFM})) \cdots\cdots \text{Equation 8}$$

However, note that if the ripple voltage in PFM mode becomes extremely small by setting a large COUT, the high-side MOSFET may turn on and switch to PWM mode before detecting 0A of inductor current during PFM mode operation.
The ripple voltage value for PFM mode to operate normally is typically 20mV or higher.

5. Designation of Phase Compensation

Since the current amplifier for the voltage feedback is output via the COMP pin, the phase compensation is achieved with using external components. The phase compensation is able to secure stable operation with using an external ceramic capacitor and the phase compensation circuit.



Connection Example for External Phase Compensation Circuit

5-1. Calculation of R_C

The phase compensation resistance (R_C) to set the calculated unity-gain frequency can be calculated by Equation 9.

$$R_C = 2 \times \pi \times \mathbf{f_{UNITY}} \times V_{OUT} \times C_{OUT_EFF} / (g_{m_ea} \times V_{REF} \times g_{m_pwr}) \cdots\cdots \text{Equation 9}$$

g_{m_ea}: Error amplifier of g_m
V_{REF}: Reference voltage (0.64V)
g_{m_pwr}: power level of g_m

$$g_{m_pwr} \times \Delta V_S = \Delta I_L$$
$$g_{m_ea} / \Delta V_S = 0.05 \times 10 \text{ ^ } (-6) \times f_{OSC} / V_{OUT}$$
$$g_{m_ea} \times g_{m_pwr} = 0.05 \times 10 \text{ ^ } (-6) \times \Delta I_L \times f_{OSC} / V_{OUT} \cdots\cdots \text{Equation 10}$$

ΔV_S: Output amplitude of the slope circuit

R_C can be calculated by substituting Equation 10 to Equation 9.

$$R_C = 2 \times \pi \times \mathbf{f_{UNITY}} \times V_{OUT} \times C_{OUT_EFF} / (V_{REF} \times 0.05 \times 10 \text{ ^ } (-6) \times \Delta I_L \times f_{OSC} / V_{OUT})$$
$$= 2 \times \pi \times 70\text{kHz} \times 3.3\text{ V} \times 100.5\mu\text{F} / (0.64 \times 0.05 \times 10 \text{ ^ } (-6) \times 2.38\text{A} \times 500\text{kHz} / 3.3\text{V})$$
$$= 12.63 \fallingdotseq 13\text{k}\Omega$$

5-2. Calculation of C_C

C_C must be calculated by Equation 11 so that the zero frequency of the error amplifier meets the highest pole frequency (f_{P_OUT}). Then, f_{P_OUT} = 5.0 kHz is determined by calculation of Equation 3.

$$C_C = 1 / (2 \times \pi \times R_C \times f_{P_OUT}) \cdots\cdots \text{Equation 11}$$
$$= 1 / (2 \times 3.14 \times 13\text{k}\Omega \times 5.0\text{kHz})$$
$$= 2.45 \fallingdotseq 2.7\text{nF}$$

5-3. Calculation of C_{C2}

C_{C2} can be calculated by two different calculation methods to vary from the zero frequency (f_{Z_ESR}) depending on the ESR of a capacitor. f_{Z_ESR} can be calculated by Equation 12.

$$f_{Z_ESR} = 1 / (2 \times \pi \times R_{COUT_ESR} \times C_{OUT_EFF}) \quad \text{Equation 12}$$
$$= 528\text{kHz}$$

[When the zero frequency is lower than $f_{OSC} / 2$]

C_{C2} sets the pole to f_{Z_ESR}

$$C_{C2} = R_{COUT_ESR} \times C_{OUT_EFF} / R_C \quad \text{Equation 13}$$

[When the zero frequency is higher $f_{OSC} / 2$]

C_{C2} sets the pole to $f_{OSC} / 2$ so as to be a noise filter for the COMP pin.

$$f_{OSC} / 2 = 1 / (2 \times \pi \times R_C \times C_{C2})$$
$$C_{C2} = 2 / (2 \times \pi \times R_C \times f_{OSC}) \quad \text{Equation 14}$$

In the reference example, C_{C2} is used as the noise filter for the COMP pin because of being higher than $f_{OSC}/2$.

$$C_{C2} = 49 \fallingdotseq 47\text{pF}$$

5-4. Calculation of C_{SPD}

C_{SPD} sets the zero frequency to meet the unity-gain frequency.

$$R_{TOP} = R_{BOT} \times (V_{OUT} / V_{REF} - 1)$$
$$C_{SPD} = 1 / (2 \times \pi \times \mathbf{f_{UNITY}} \times R_{TOP}) \quad \text{Equation 15}$$

When $R_{BOT} = 22\text{k}\Omega$

$$R_{TOP} = 22\text{k} \times (3.3\text{V} / 0.64\text{V} - 1)$$
$$= 91.4\text{k}\Omega$$

$$C_{SPD} = 1 / (2 \times \pi \times 70\text{kHz} \times 91.4\text{k}\Omega)$$
$$= 24.8 \fallingdotseq 27\text{pF}$$

● Cautions in Selecting External Components

Inductor

- Choose an inductor that has small DC resistance, has sufficient allowable current and is hard to cause magnetic saturation. The inductance value must be determined with consideration of load current under the actual condition. If the inductance value of an inductor is extremely small, the peak current of SW may increase along with the load current. As a result, the current limit circuit may start to operate when the peak current of SW reaches to "SW limit current".

Capacitor

- Choose a capacitor that has a sufficient margin to the drive voltage ratings with consideration of the DC bias characteristics and the temperature characteristics.
- The use of a ceramic capacitor for C_{IN} is recommended. If combined use of a ceramic and the electrolyte capacitor, the stable operation will improve since the margin becomes bigger. Choose the electrolyte capacitor with the lowest possible ESR with consideration of the allowable ripple current rating (I_{RMS}). I_{RMS} can be calculated by the following equation.

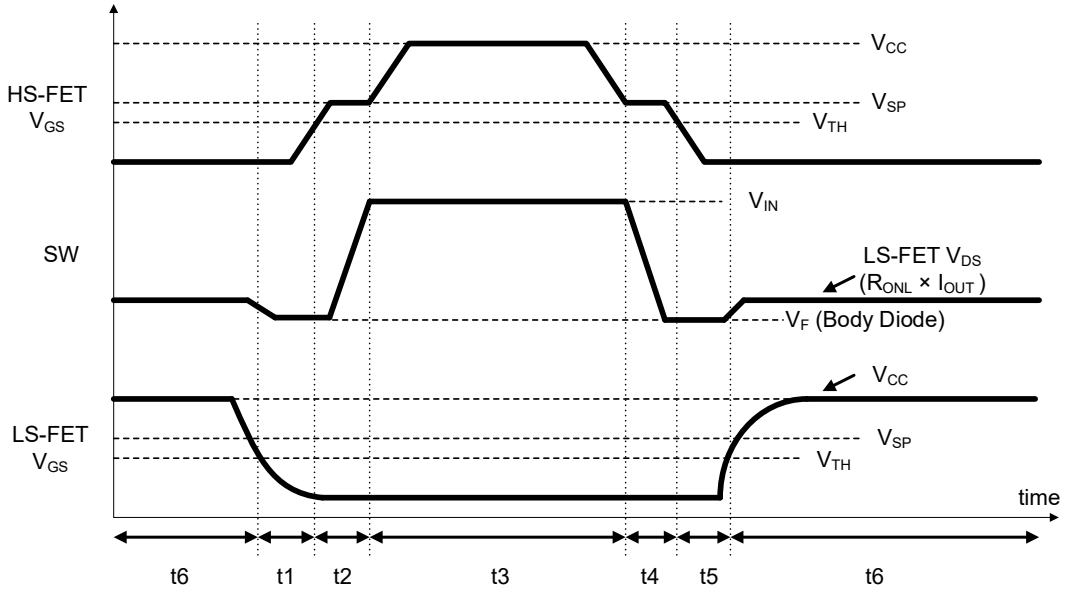
$$IRMS \fallingdotseq I_{OUT} / V_{IN} \times \sqrt{\{ V_{OUT} \times (V_{IN} - V_{OUT}) \}}$$

MOSFET

- Gate - Source Voltage
  When considering variations in production and margin, a MOSFET with a withstand voltage of 10 V or more is recommended despite the 5 V high and low driver.
- Gate Threshold Voltage
  Choose a MOSFET with the threshold voltage between 1.0 V (Min.) and 3.4 V (Max.) with consideration of variations in production and margin.
- Drain Current
  Choose a MOSFET having a sufficient margin with consideration of peak current and limit current.
- Connection of Body Diode for Source Current
  Choose a diode with the withstand current over the reverse limit current rating. The NC2780 reverse current value becomes one-half of the normal limit current value.
- Input Capacitor (C_{ISS})
  As an index of performance, C_{ISS}: 3800pF
- On-resistance (R_{DS} (on)) & All Gate Capacitance (Qg)
  Choose a MOSFET with the lowest possible characteristics because having an influence on efficiency. Generally, a high-performance MOSFET is rated that R_{DS} x Qq (performance figure) is small.
- Since test specifications vary with MOSFET makers, it is necessary to confirm the application with the NC2780 implemented on a board system.

MOSFET Losses

The MOSFET total loss is calculated by the sum of the switching losses when the high-side and the low-side MOSFETs turning-on / off and the conduction losses by the MOSFET's on-resistance. If the total loss become larger than expected, the external MOSFET must be selected with consideration of the on-resistance, the switching losses and the package's power dissipation. The following figure shows the timing chart of the high side / low side MOSFETs at normal switching. The loss at each delay time can be calculated as follows.



DC / DC Converter Basic Switching Timing Chart

t1 (t5):

For the duration between the low-side MOSFET's turn-off and the high-side MOSFET's turn-on, the loss occurs to supply a current from the body diode on the low-side MOSFET. Likewise, for the duration between the high-side MOSFET's turn-off and the low-side MOSFET's turn-on, the loss occurs. The losses (P_{DEAD}) for t1 and t5 can be calculated by the following equation.

$$P_{DEAD} = V_F \times I_{OUT} \times f_{OSC} \times (t_{DEAD1} + t_{DEAD5})$$

V_F: The forward voltage of a body-diode

t_{DEAD1}: The delay time from the instant when the gate-source voltage (V_{GS}) falls below the threshold voltage (V_{TH}) on the low-side MOSFET to the instant when V_{GS} exceeds V_{TH} on the high-side MOSFET.

T_{DEAD5}: The delay time from the instant when V_{GS} falls below V_{TH} on the high-side MOSFET to the instant when V_{GS} exceeds V_{TH} on the low-side MOSFET.

t2 (t4):

Since the drain-source voltage (V_{DS}) is equal to V_{IN} when the high-side MOSFET turns on/off after delay time ($t_{DEAD}1$ / t_{DEAD5}), the source current and the output current (I_{OUT}) become equal. Therefore, a large loss occurs. The losses (P_{SW}) at turn-on / off can be calculated by the following equation.

$$P_{SW} = 1/2 \times V_{IN} \times I_{OUT} \times f_{OSC} \times (t_{RISE} + t_{FALL})$$

t_{RISE}: A duration between the gate voltage rising start time from the threshold voltage and the end of stabilized voltage (V_{SP}) on the high-side MOSFET.

T_{FALL}: A duration between the start time of the gate voltage stabilizing and the falling time below the threshold voltage on the high-side MOSFET.

For the stabilized duration, V_{GS} of the high-side MOSFET remains constant roughly since the gate charge current is used to charge C_{GD}. And, the reverse recovery loss (P_{RR}) occurs to recover the body diode of the low-side MOSFET when the high-side MOSFET turns on. Refer to *the MOSFET datasheet* for information about the electric charge (Qrr) required for recovery.

$$P_{RR} = V_{IN} \times Qrr \times f_{OSC}$$

And, the power (P_{GH}, P_{GL}) for electric charge of the MOSFET' gate and the power (P_{OSSH}, P_{OSSL}) for electric charge of the MOSFET's output capacity occur. Each power can be calculated by following equations. Refer to *the MOSFET datasheet* for detailed values.

$P_{GH} = Q_{GH} \times V_{CC} \times f_{OSC}$
$P_{GL} = Q_{GL} \times V_{CC} \times f_{OSC}$
$P_{OSSH} = 1/2 \times C_{OSSH} \times (V_{IN})^2 \times f_{OSC}$
$P_{OSSL} = 1/2 \times C_{OSSL} \times (V_{IN})^2 \times f_{OSC}$

V_{CC}: VCC pin voltage
Q_{GH}, Q_{GL}: Gate electric charge quantity for High- /Low- side MOSFETs
C_{OSSH}, C_{OSSL}: Drain-gate capacity + Drain-source capacity for High- /Low- side MOSFETs

t3 (t6):
For the duration of t3, the conduction loss of the high-side MOSFET (P_{HS}(on)) occurs. For the duration of t6, the conduction loss of the low-side MOSFET (P_{LS}(on)) occurs. Each loss can be calculated by the following equation. ON duty is closely analogous to V_{OUT} / V_{IN}.

$I_{RMS} = \sqrt{}\ (((I_{OUT})^2 + (I_{P-P})^2 / 12))$
P_{HS} (on) = $(I_{RMS})^2 \times R_{ONH} \times V_{OUT} / V_{IN}$
P_{LS} (on) =$(I_{RMS})^2 \times R_{ONL} \times (1\text{-}V_{OUT} / V_{IN})$

I_{RMS}: MOSFET's rms current
I_{P-P}: MOSFET's peak current amplitude
R_{ONH}, R_{ONL}: On-resistance for High- /Low- side MOSFETs

Since the conduction loss depends on the duty, the loss varies with step-down ratio. When the step-down ratio is large and the ON duty is small, the loss of the low side MOSFET becomes larger, and when the ratio is small, the loss of the high-side MOSFET becomes larger. From above equations, each loss of the high-side and the low-side MOSFETs can be calculated by the following equations.

$P_{HS} = P_{HS}$ (on) + P_{SW} + P_{RR} + P_{GH} + P_{OSSH}
$P_{LS} = P_{LS}$ (on) + P_{GL} + P_{OSSL} + P_{DEAD}

As is evident from these equations, the switching loss becomes predominant when the input voltage and the frequency are high, and the conduction loss conversely becomes predominant when they are low.

● Technical Notes

The performance of power source circuits using this IC largely depends on peripheral circuits. When selecting the peripheral components, please consider the conditions of use. Do not allow each component, PCB pattern or the IC to exceed their respected rated values (voltage, current, and power) when designing the peripheral circuits.

- It is recommended to mount all the external components on the same layer as the IC on board. External components must be connected as close as possible to the Ics and make wiring as short as possible. Especially, the capacitor connected in between VIN pin and GND pin must be wiring the shortest. If their impedance is high, internal voltage of the IC may shift by the switching current, and the operating may be unstable. Make the power supply and GND lines sufficient.

- Since the current loop of a switching regulator changes with each switching, the current changes significantly and high-frequency noise may be generated due to parasitic capacitance and inductance. Design the board layout so that the current loop length is as short as possible.

- AGND and PGND for the controller must be wired to the GND line at the low impedance point of the same layer with C_{IN} and C_{OUT}. Reduce the impedance between the AGND and PGND of IC.

- It is recommended that the C_{IN}, high-side, and low-side MOSFETs be placed on the same layer as the IC on PCB. If vias are used and placed on a different layer from the IC, the parasitic inductance of vias may affect the ringing of the SW pin voltage and increase noise.

- R_{TOP}, R_{BOT}, and C_{SPD} should be set close to the FB pin, but mount them away from the inductor, SW pin, and BST pin to avoid their noise.

- Place a capacitor (C_{BST}) as close as possible to the SW pin and the BST pin. If controlling slew rate for EMI, a resistor (R_{BST}) should be in series between the BST pin and the capacitor (C_{BST}), but not be in series to MOSFET for HGATE and LGATE pins. Because connecting the resistor in series to the MOSFET becomes a cause of a through-current.

- The tab on the bottom of the HSOP-18-AK package must be connected to GND when mounted on the board. To improve thermal dissipation on the multilayer board, set via to release the heat to the other layer in the connecting part of the tab on the bottom. Likewise, thermal dissipation for MOSFET is required.

- The MODE pin requires the “High” / “Low” voltages with the high stability when the forced PWM mode (MODE = “High”) or the PFM mode (MODE = “Low”) is enabled. If the voltage with the high stability cannot be applied, connection to the VCC pin as “High” level or the AGND pin as “Low” level is recommended. If connecting to the PGND pin as noisy, a malfunction may occur. Avoid the use of the MODE pin being “Open”.

- If V_{OUT} is a minus potential, the setup cannot occur.

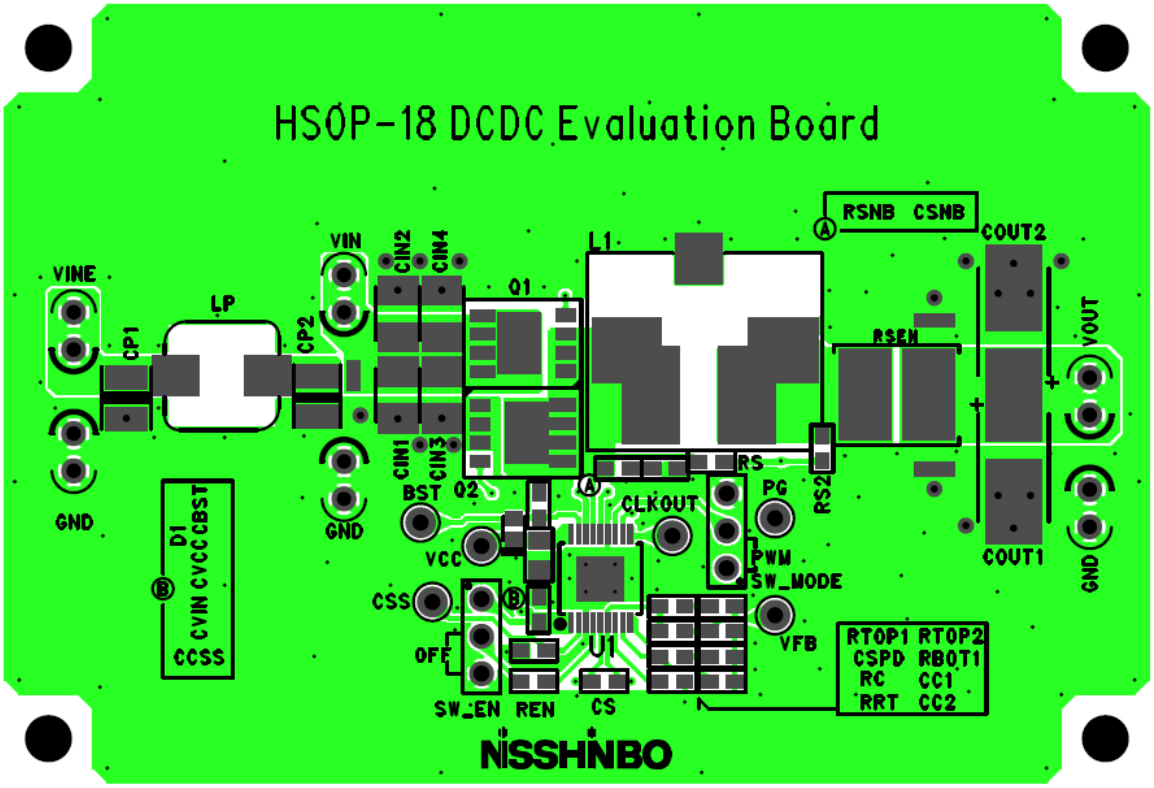
- The power for the controller and for the high-side MOSFET must be used on the same power supply, since the internal slope compensation is applied as the power supply voltage of the high-side MOSFET is equal to the controller’s. If applying the other power supply voltage, the controller will become unstable owing to the inappropriate slope compensation.

- The thermal shutdown function prevents the IC from fuming and ignition but does not ensure the IC’s reliability or keep the IC below the absolute maximum ratings. The thermal shutdown function does not operate on the heat generated by other than the normal IC operation such as latch-up and overvoltage application.

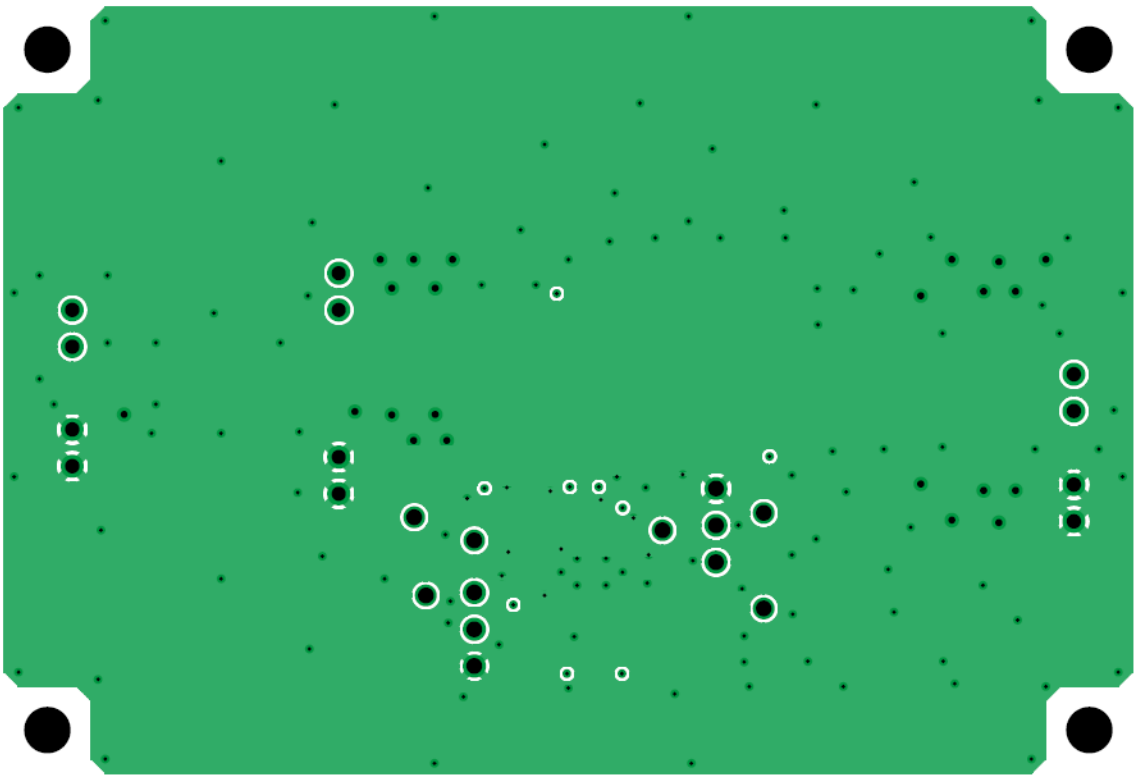
- The thermal shutdown function operates in a state over the absolute maximum ratings, therefore the thermal shutdown function should not be used for a system design.

REFERENCE PCB LAYOUTS

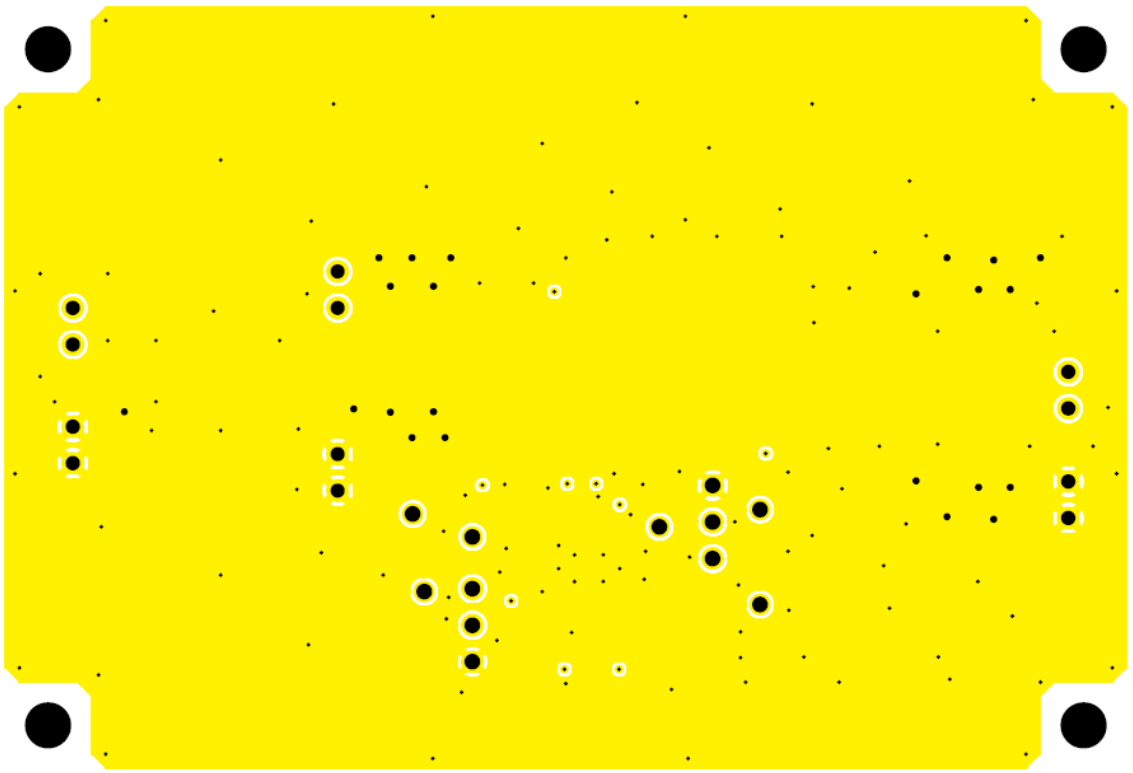
NC2780 PCB Layouts



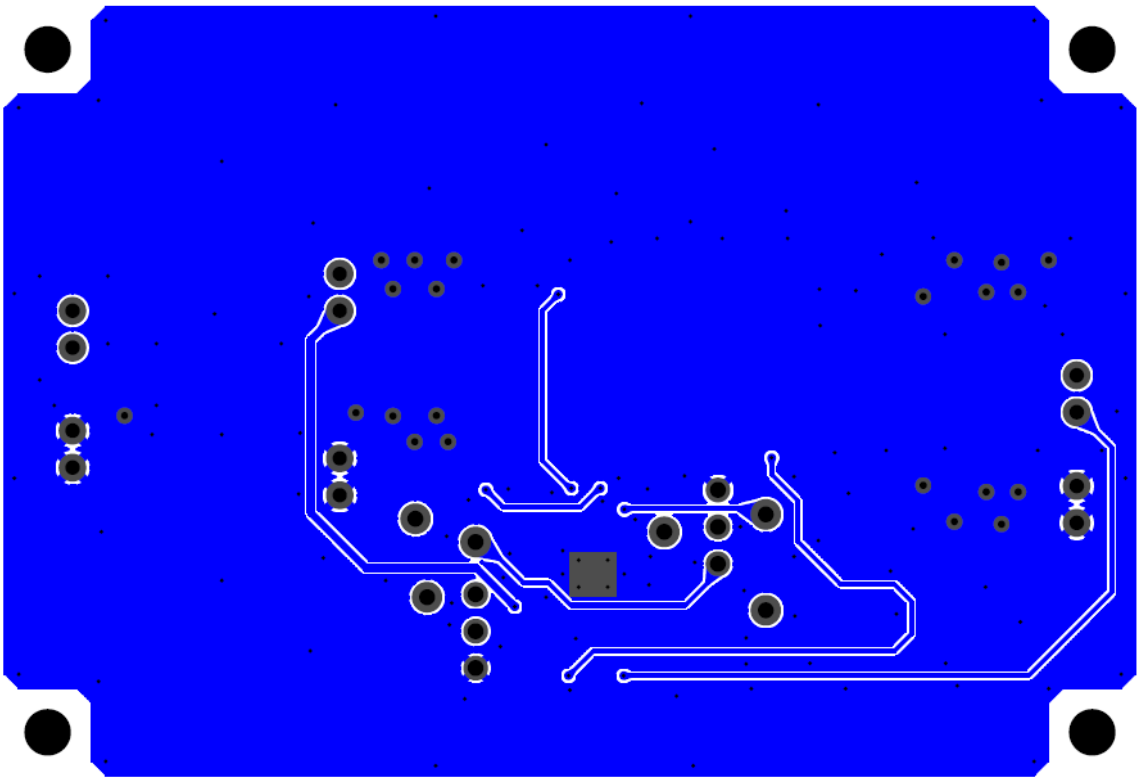
PCB Layout - 1st Layer (Top Layer)



PCB Layout - 2nd Layer

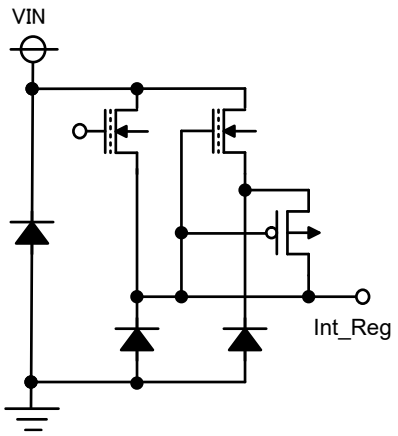


PCB Layout - 3rd Layer

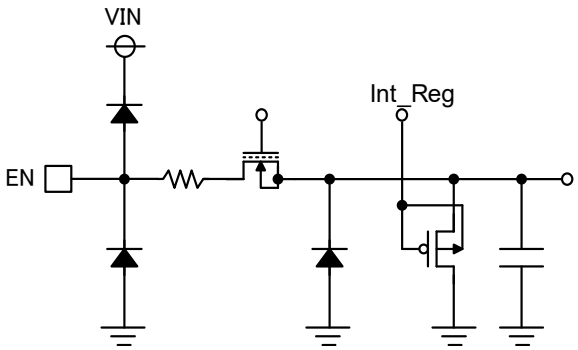


PCB Layout - 4th Layer (Bottom Layer)

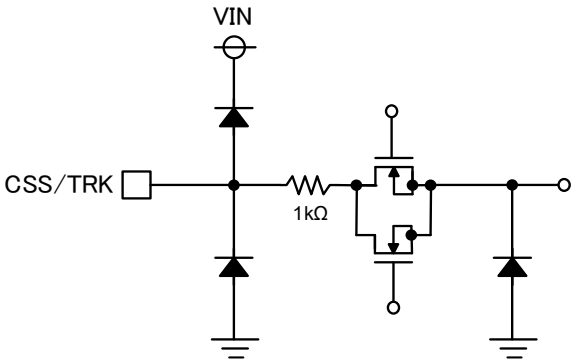
INTERNAL EQUIVALENT CIRCUIT FOR EACH PIN



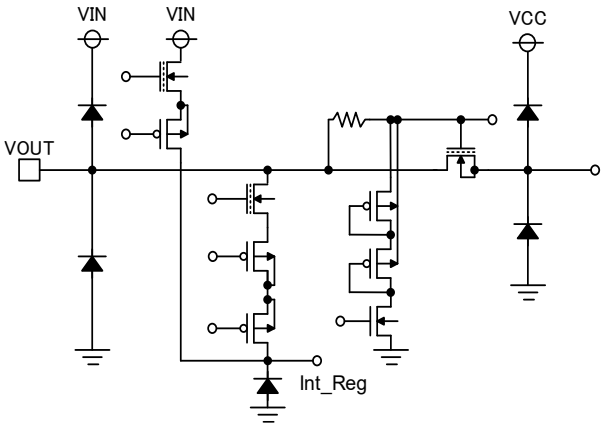
VIN Pin



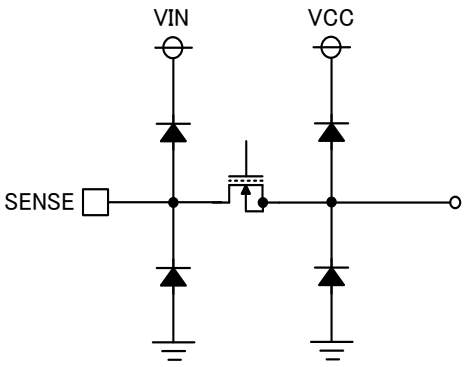
EN Pin



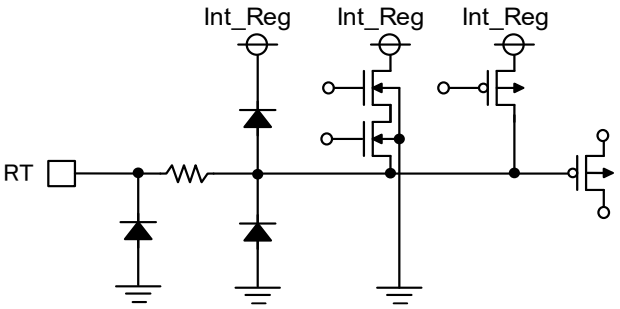
CSS/TRK Pin



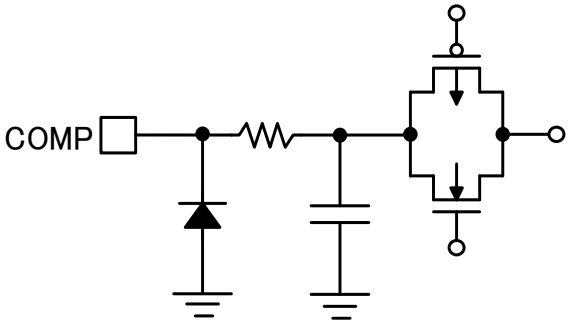
VOUT Pin



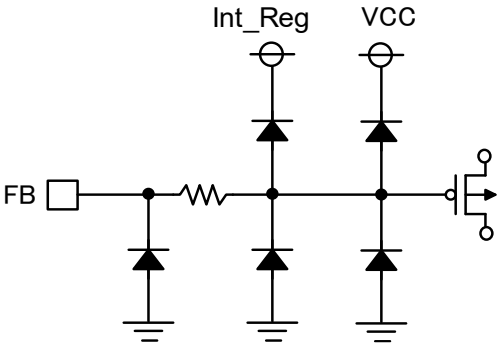
SENSE Pin



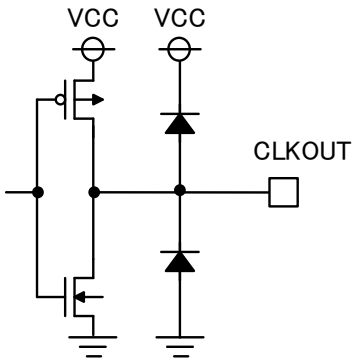
RT Pin



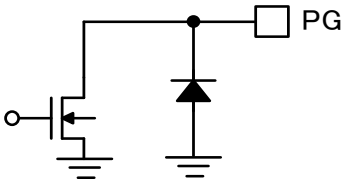
COMP Pin



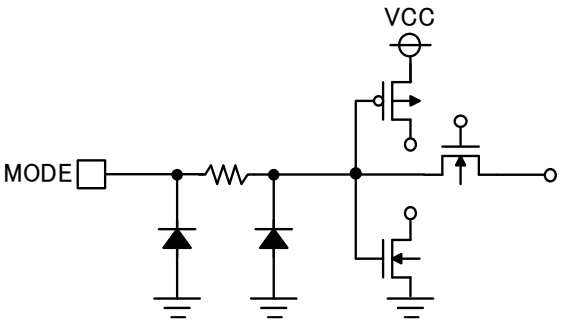
FB Pin



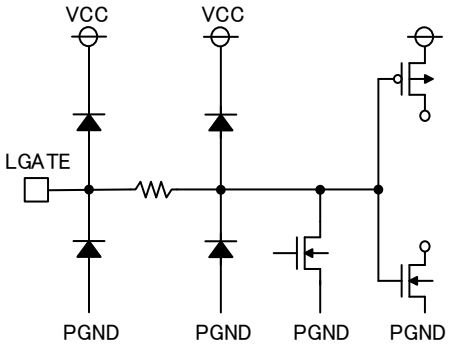
CLKOUT Pin



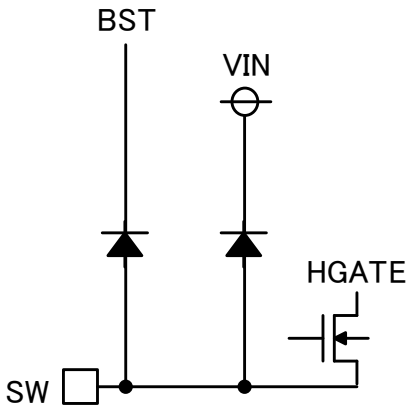
PG Pin



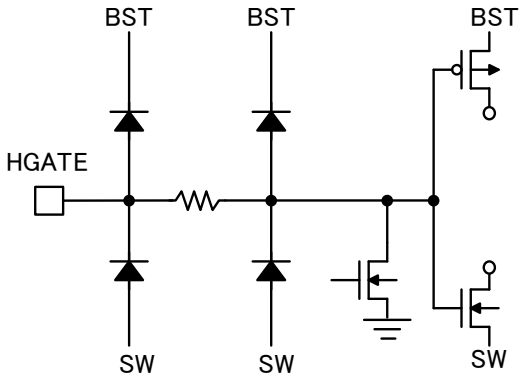
MODE Pin



LGATE Pin

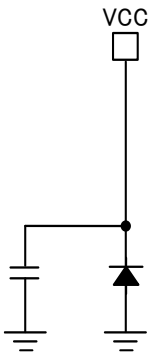


SW Pin

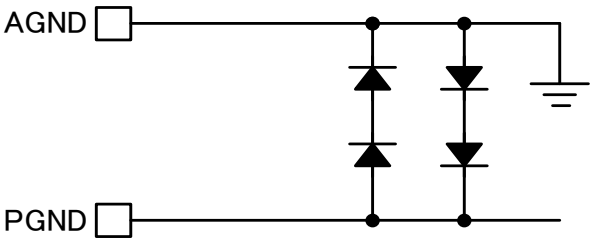


HGATE Pin

BST Pin



VCC Pin



AGND - PGND Pins

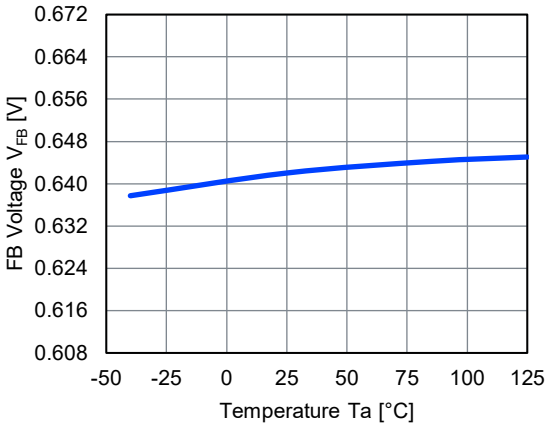
TYPICAL CHARACTERISTICS

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

V_{IN} = 12 V, NC2780AK001B, Ta = 25 °C

1) FB Voltage vs Temperature

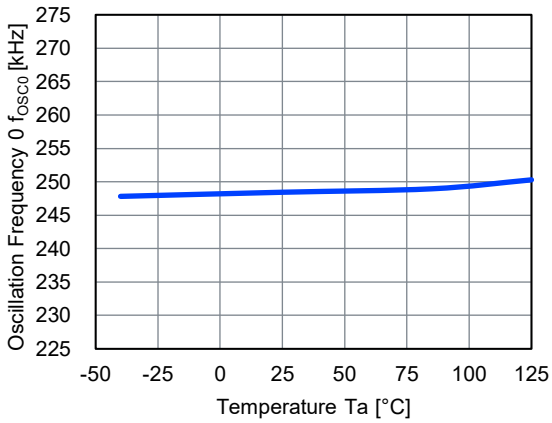
MODE = "High"



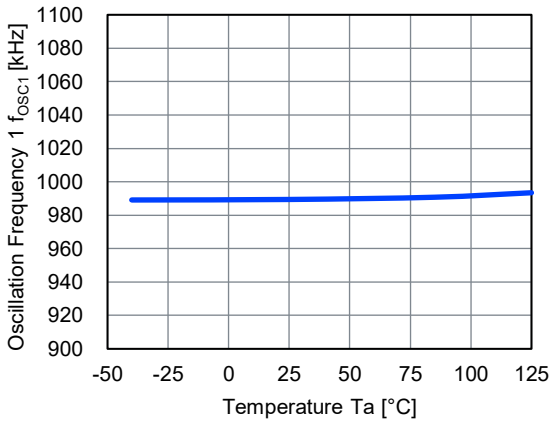
2) Oscillation Frequency vs Temperature

MODE = "High"

F_{OSC} = 250 kHz

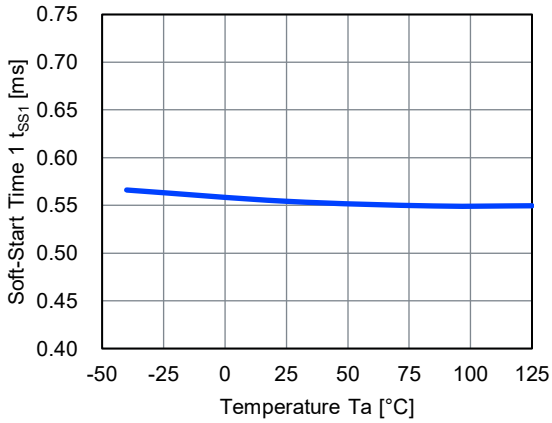


F_{OSC} = 1000 kHz

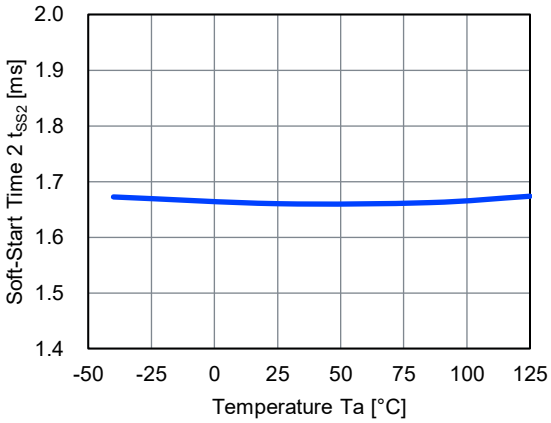


3) Soft-Start Time vs Temperature

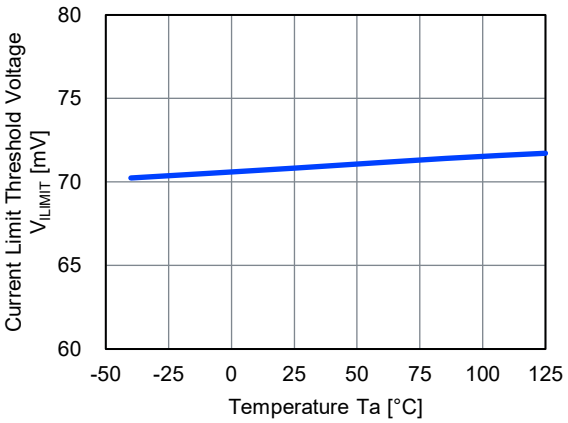
C_{SS} = none



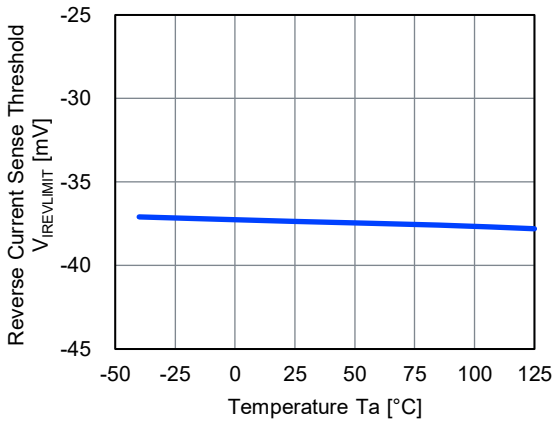
C_{SS} = 4.7 nF



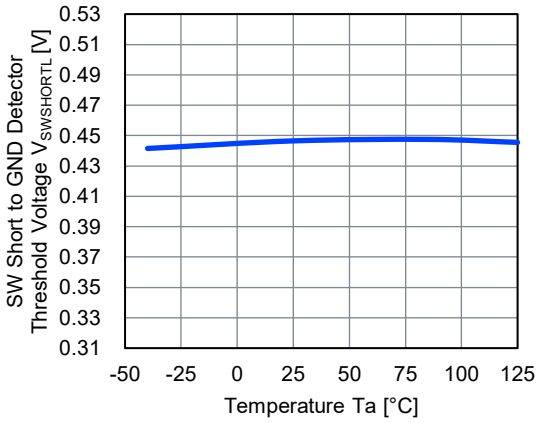
4) Current Limit Threshold Voltage vs Temperature
NC2780AKxxx2x, MODE = “High”
Current Limit Threshold Voltage



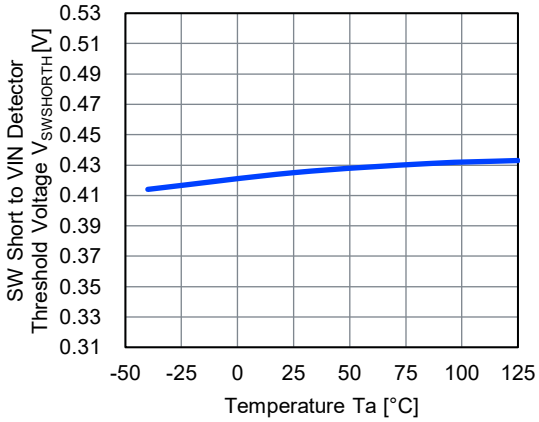
Reverse Current Sense Threshold Voltage



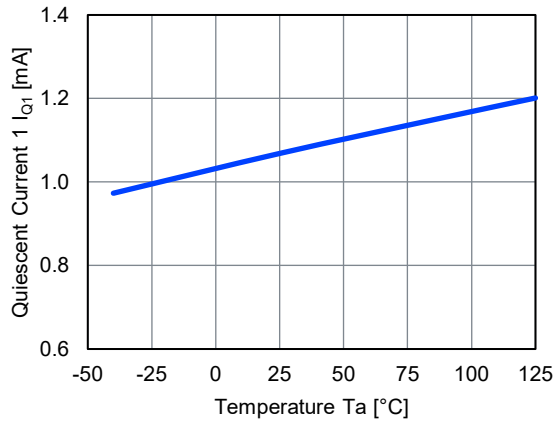
5) SW Ground Short Threshold Voltage vs Temperature
MODE = “High”



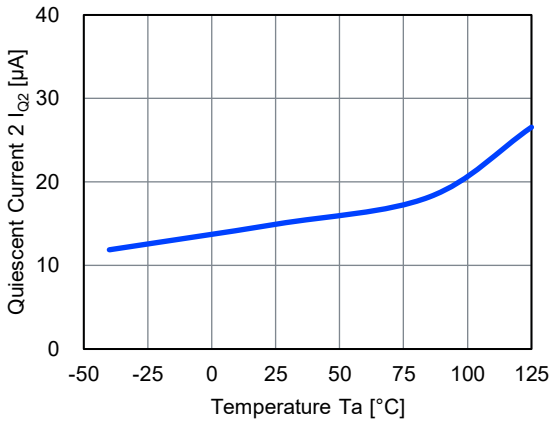
6) VIN Short Detection Threshold Voltage vs Temperature
MODE = “High”



7) Quiescent Current vs Temperature
NC2780AK0xxx
V_{OUT} = 5 V
MODE = “High”

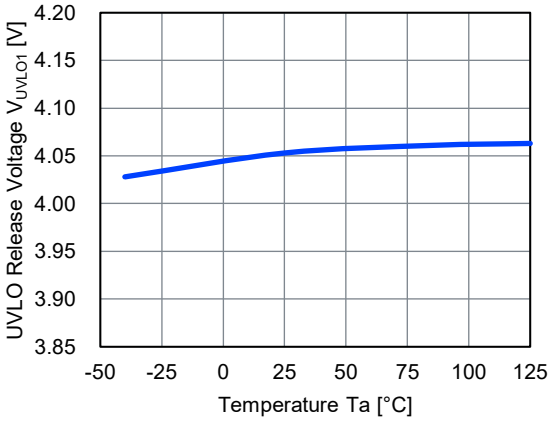


MODE = “Low”

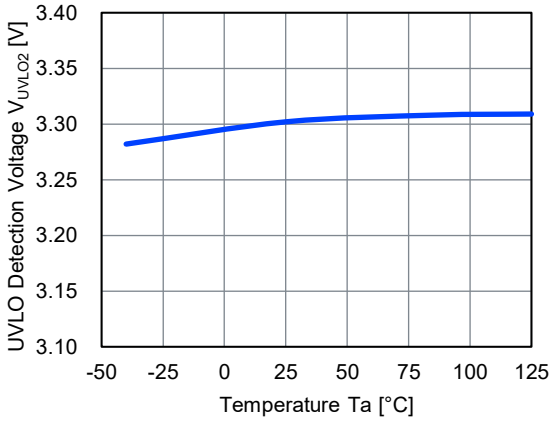


8) UVLO Threshold Voltage vs Temperature

Release

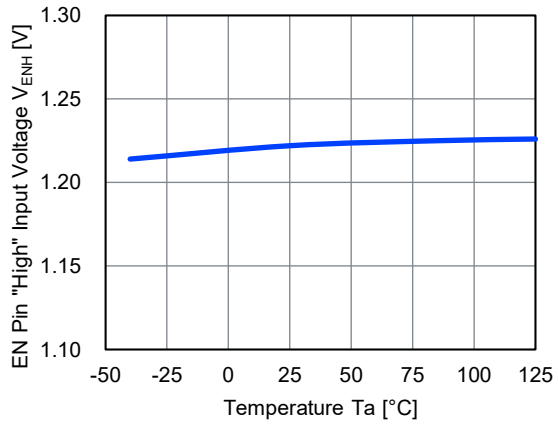


Detect

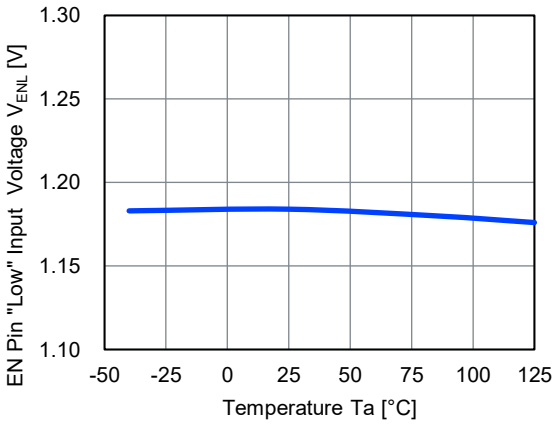


9) EN Input Voltage vs Temperature

EN = “High”

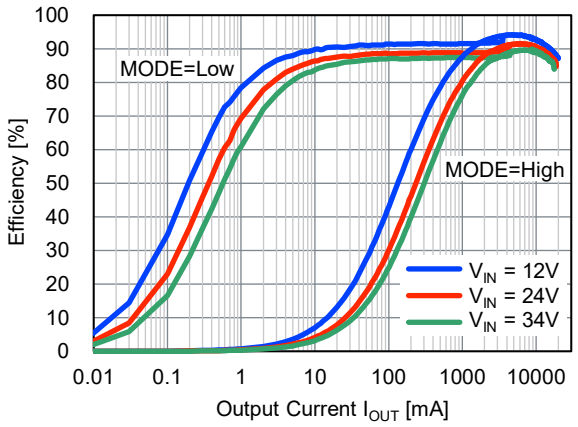


EN = “Low”

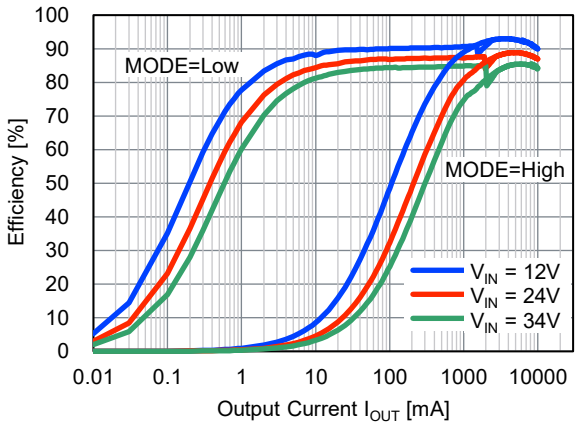


10) Efficiency vs Output Current

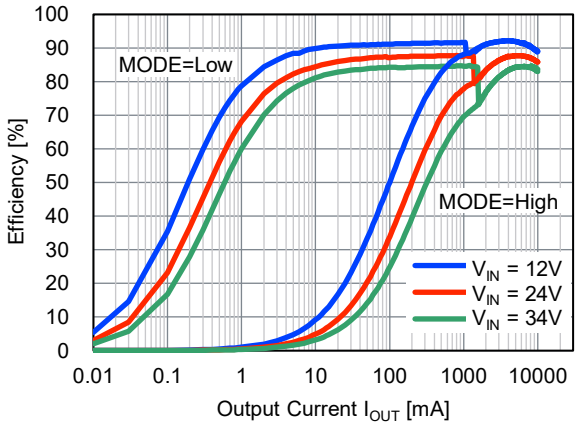
V_{OUT} = 3.3 V
F_{OSC} = 250 kHz



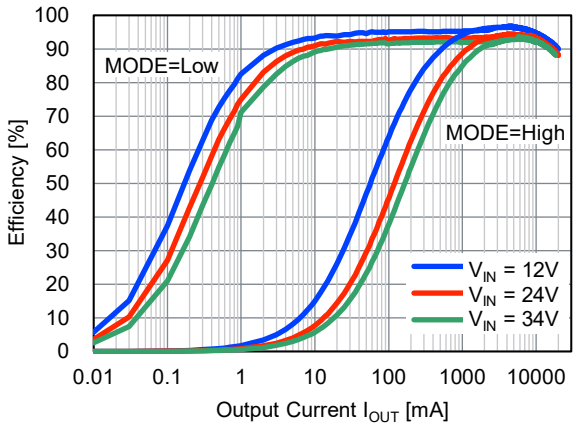
F_{OSC} = 500 kHz



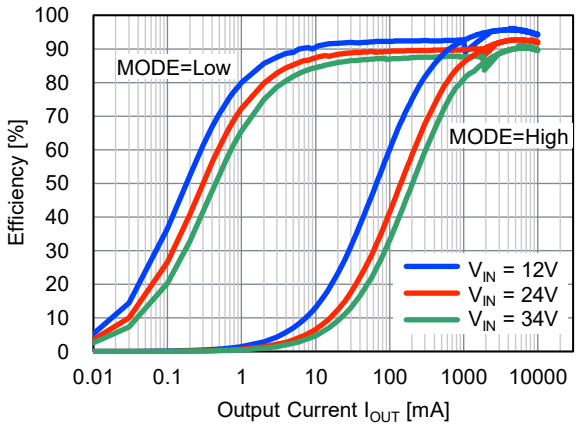
F_{OSC} = 1000 kHz



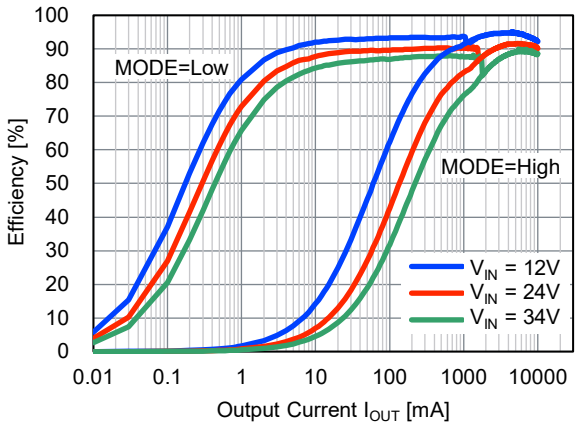
V_{OUT} = 5 V
F_{OSC} = 250 kHz



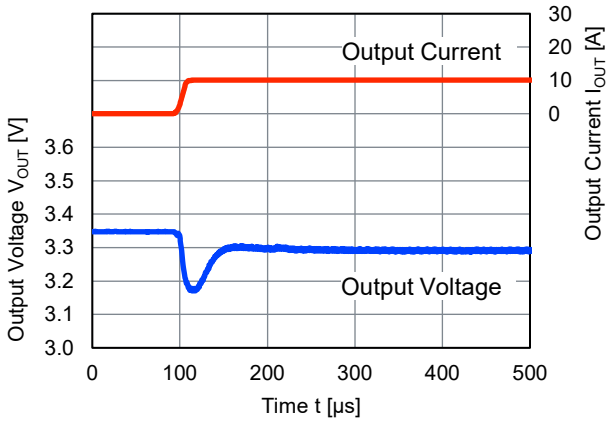
F_{OSC} = 500 kHz



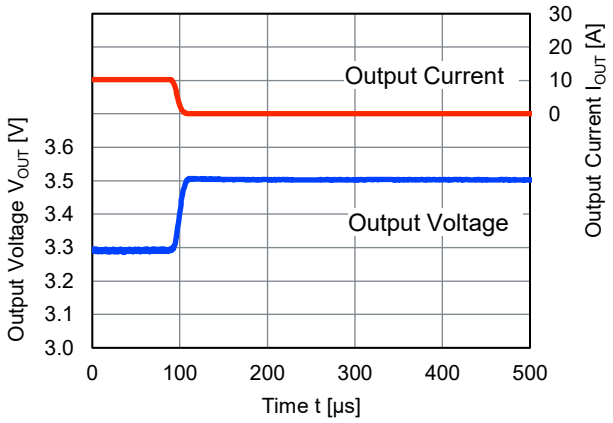
F_{OSC} = 1000 kHz



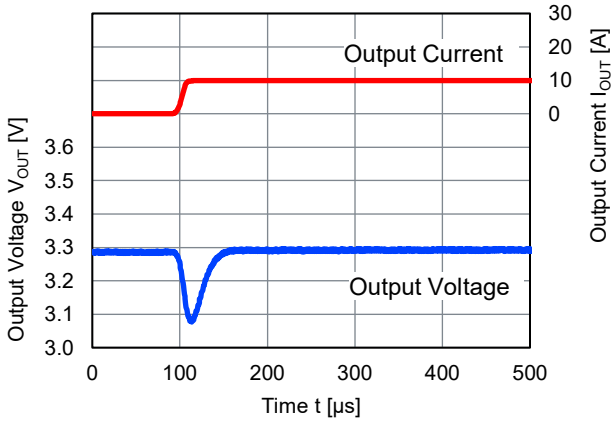
11) Load Transient Response
V_{OUT} = 3.3 V, F_{OSC} = 500 kHz
MODE = "Low"
I_{OUT} = 0 A to 10 A



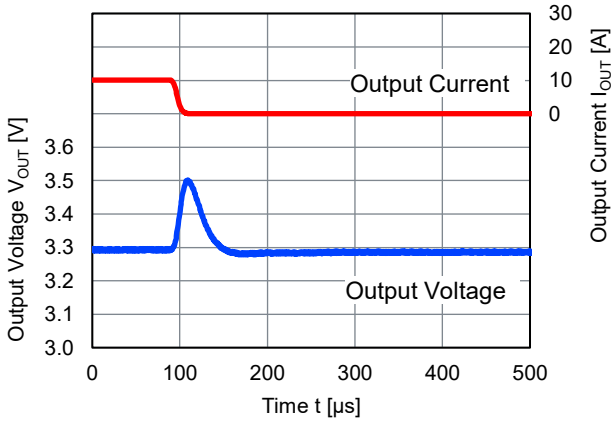
I_{OUT} = 10 A to 0 A



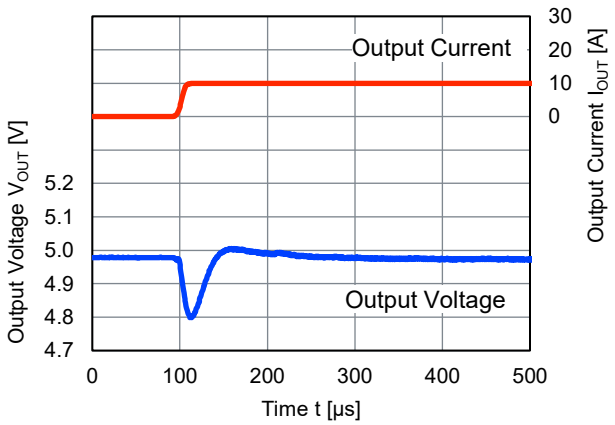
MODE = "High"
I_{OUT} = 0 A to 10 A



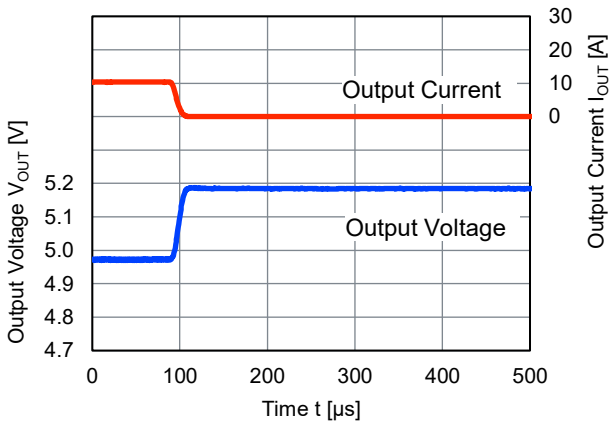
I_{OUT} = 10 A to 0 A



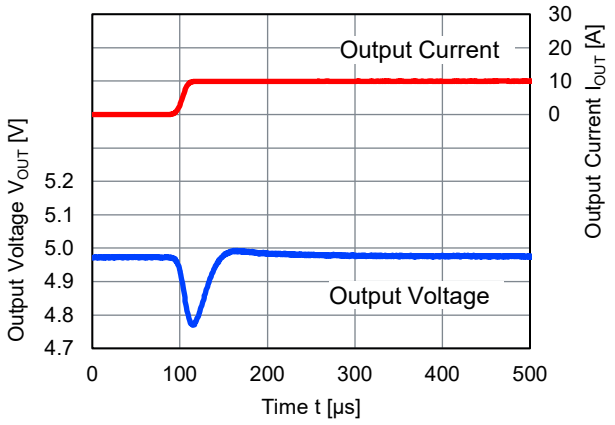
V_{OUT} = 5 V, F_{OSC} = 500 kHz
MODE = “Low”
I_{OUT} = 0 A to 10 A



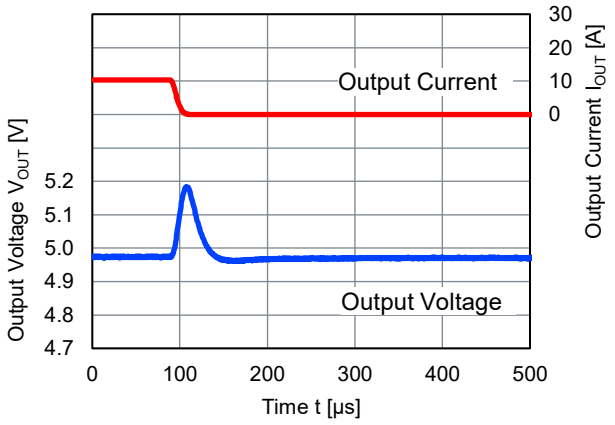
I_{OUT} = 10 A to 0 A



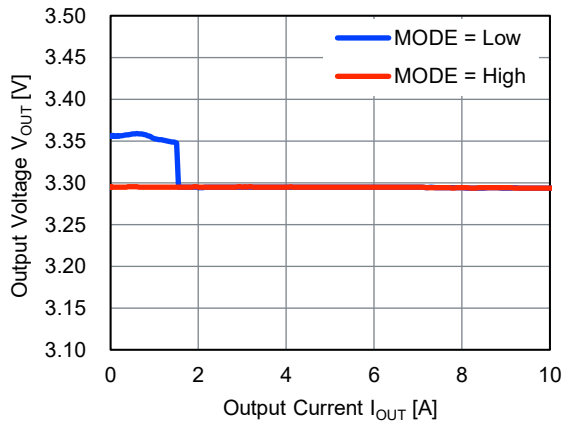
MODE = “High”
I_{OUT} = 0 A to 10 A

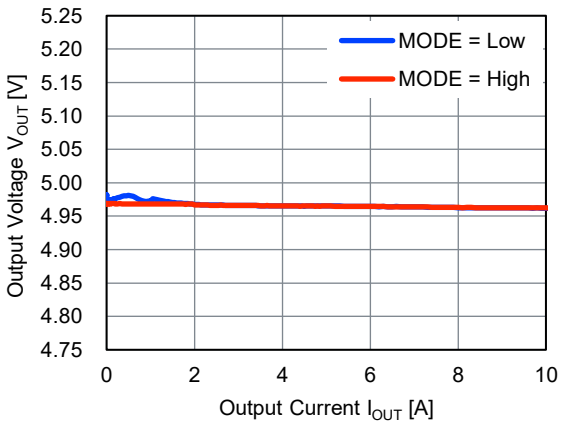


I_{OUT} = 10 A to 0 A

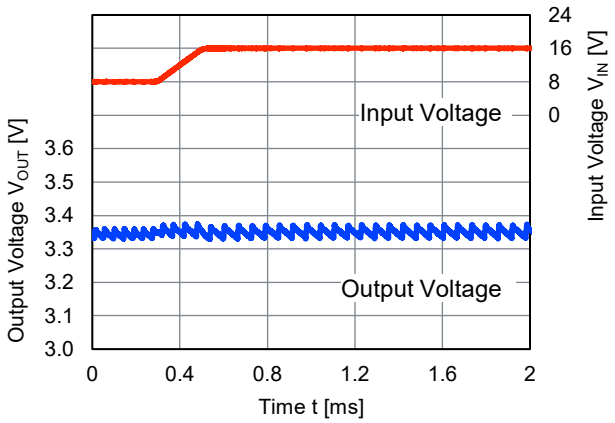


12) Load Regulation
V_{OUT} = 3.3 V, F_{OSC} = 500 kHz

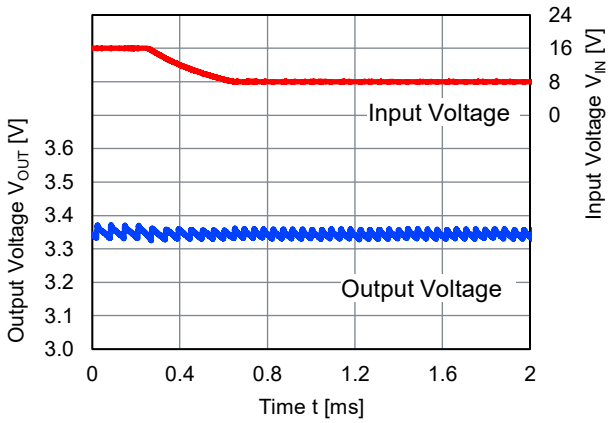




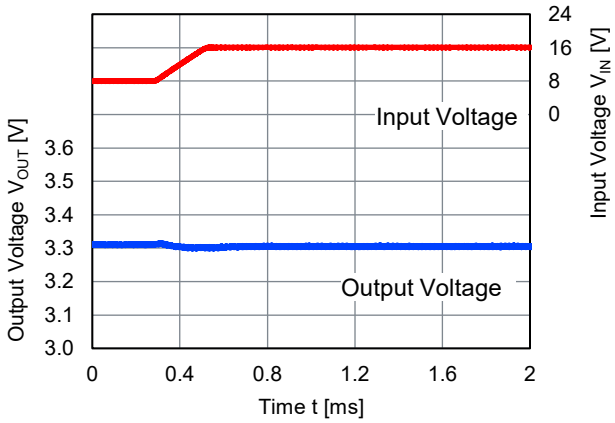
13) Line Transient Response
V_{OUT} = 3.3 V, F_{OSC} = 500 kHz
MODE = "Low", I_{OUT} = 0.1 A
V_{IN} = 8 V to 16 V



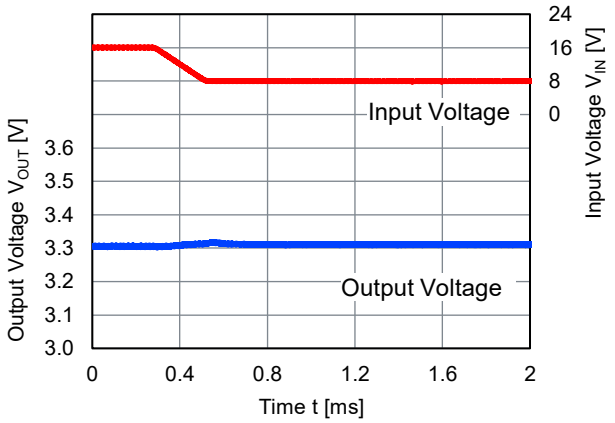
V_{IN} = 16 V to 8 V



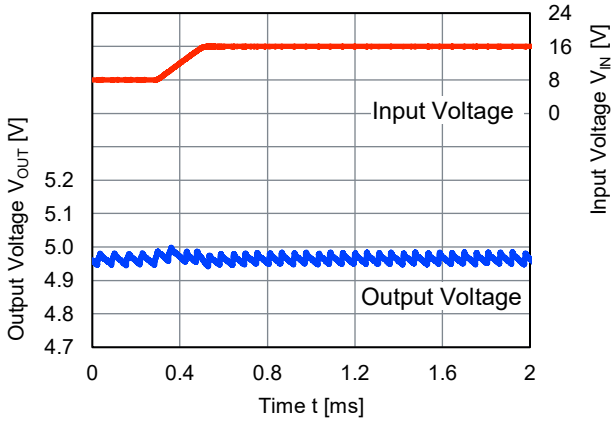
MODE = "High", I_{OUT} = 10 A
V_{IN} = 8 V to 16 V



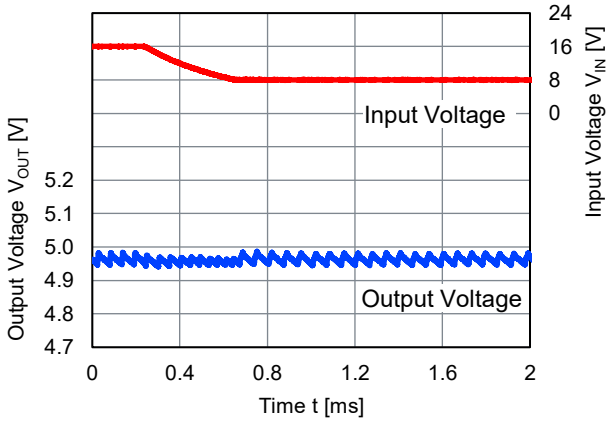
V_{IN} = 16 V to 8 V



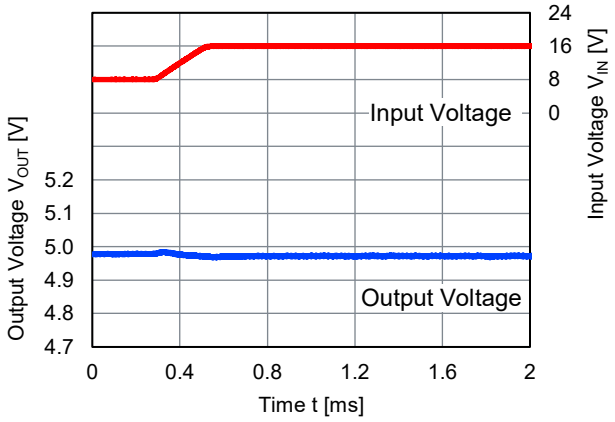
V_{OUT} = 5 V, F_{OSC} = 500 kHz
MODE = "Low", I_{OUT} = 0.1 A
V_{IN} = 8 V to 16 V



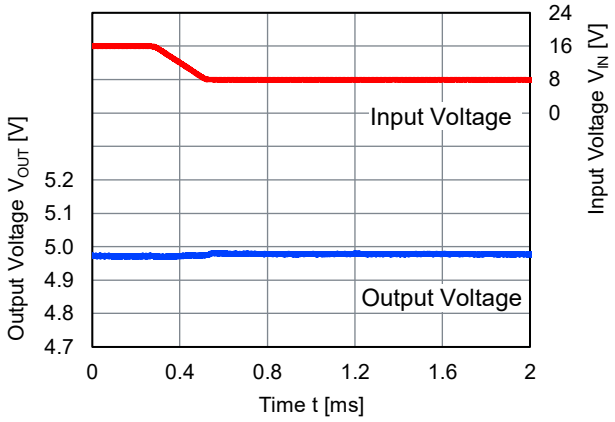
V_{IN} = 16 V to 8 V



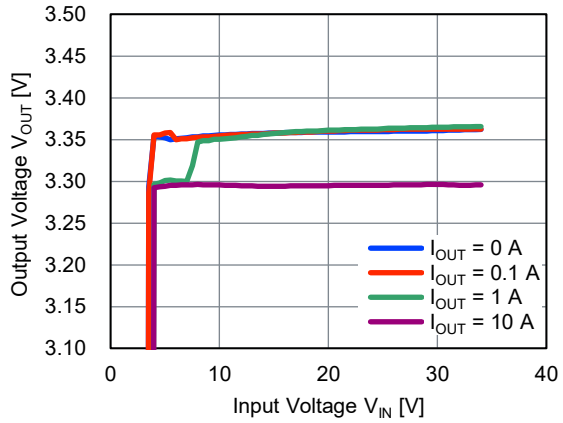
MODE = “High”, I_{OUT} = 10 A
V_{IN} = 8 V to 16 V



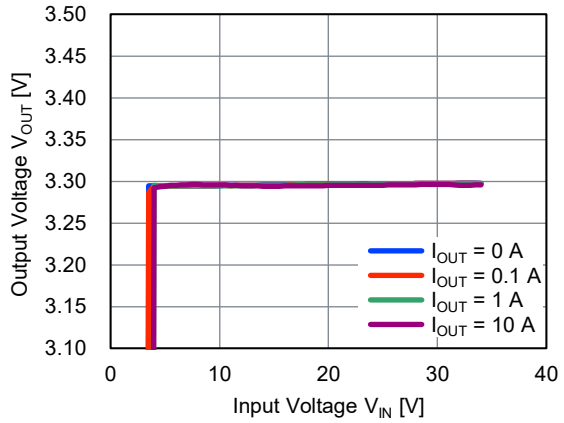
V_{IN} = 16 V to 8 V



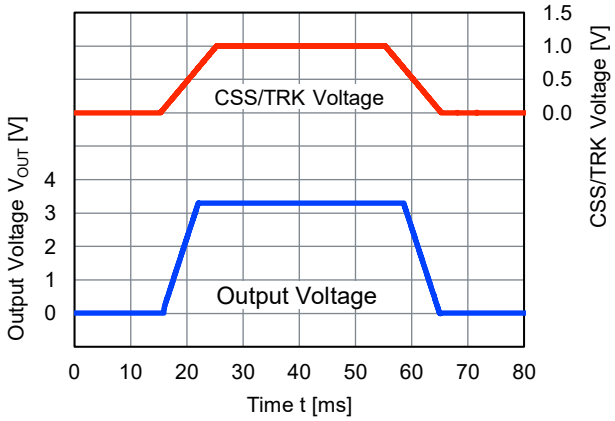
14) Line Regulation
V_{OUT} = 3.3 V, F_{OSC} = 500 kHz
MODE = “Low”



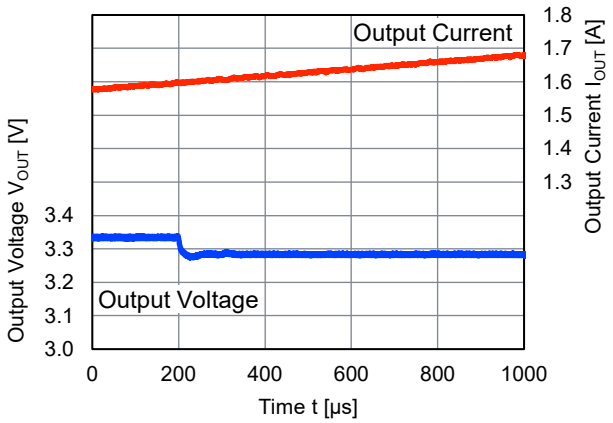
MODE = “High”



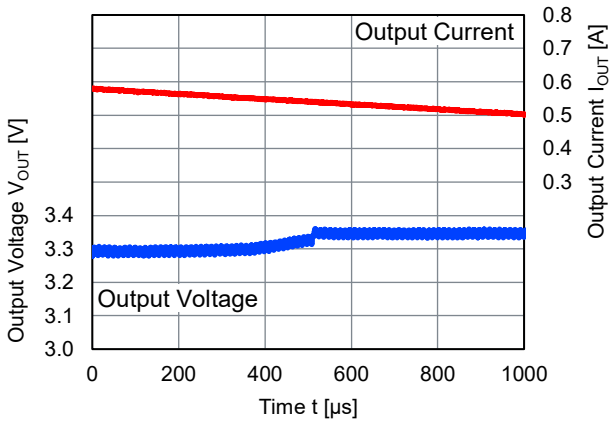
15) Up – Down Tracking
V_{OUT} = 3.3 V, F_{OSC} = 500 kHz, I_{OUT} = 0 A, MODE = “High”



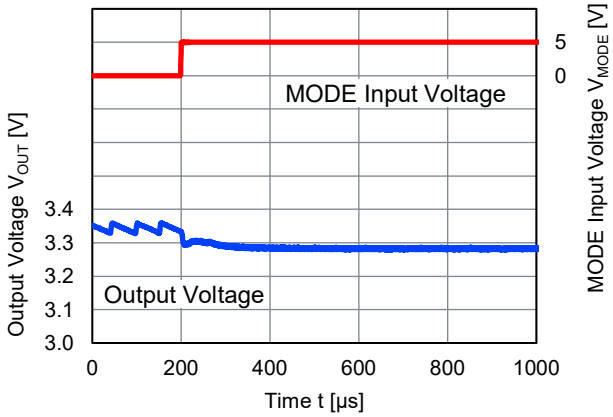
16) MODE Transient Response
V_{OUT} = 3.3 V, F_{OSC} = 500 kHz
MODE = "Low"
I_{OUT} = SweepUp



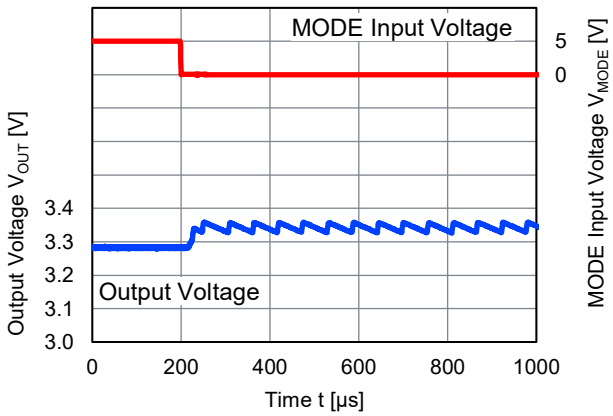
I_{OUT} = SweepDown



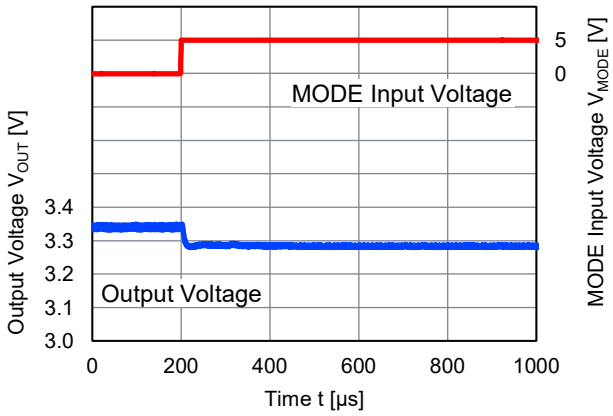
I_{OUT} = 0.1 A
MODE = "Low" to "High"



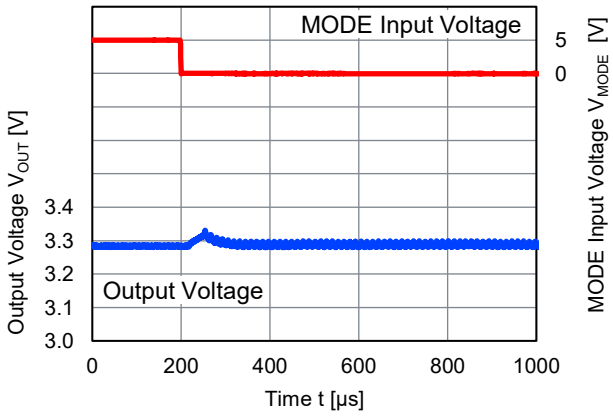
MODE = "High" to "Low"



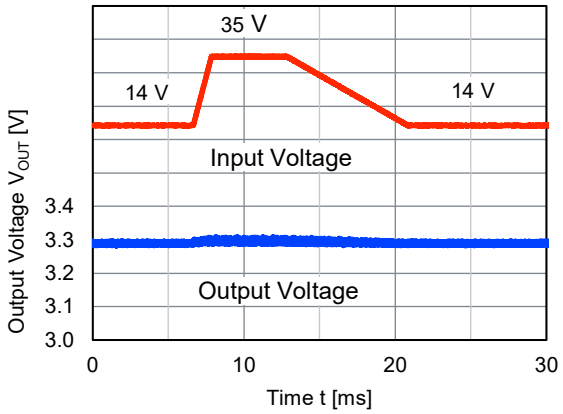
I_{OUT} = 1 A
MODE = "Low" to "High"



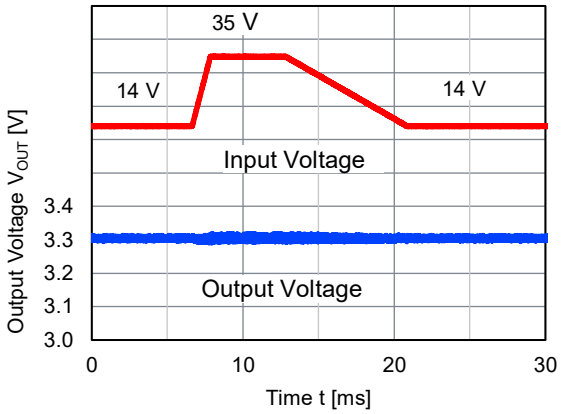
MODE = "High" to "Low"



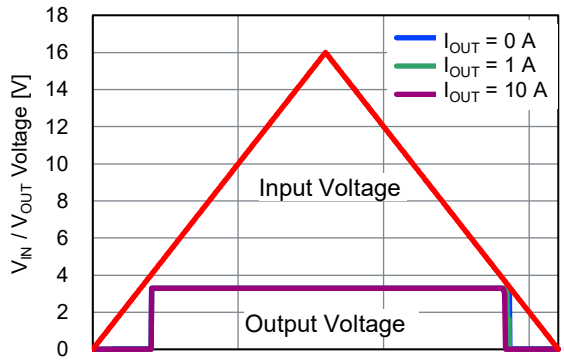
17) Load Dump
V_{OUT} = 3.3 V, F_{OSC} = 500 kHz
MODE = "High"
I_{OUT} = 0 A



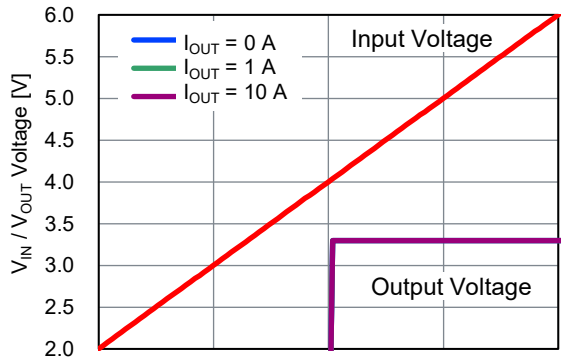
I_{OUT} = 10 A



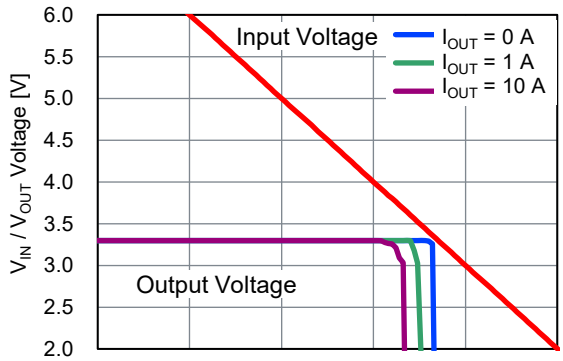
18) Dropout Voltage
V_{OUT} = 3.3 V, F_{OSC} = 250 kHz, MODE = "High"
V_{IN} = 0 V to 16 V to 0 V



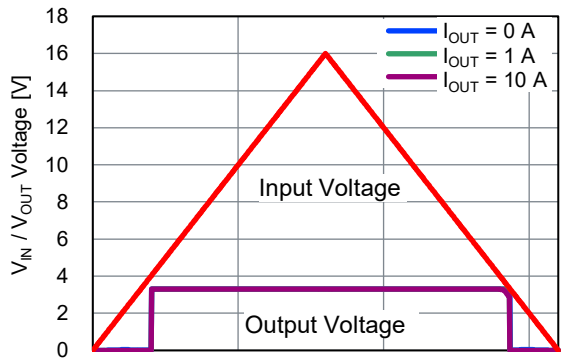
UVLO Release Voltage Zoom-in View



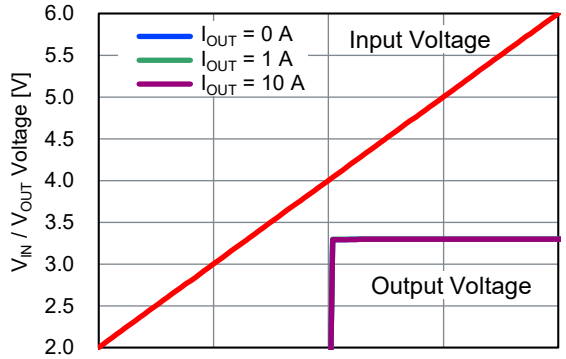
UVLO Detection Voltage Zoom-in View



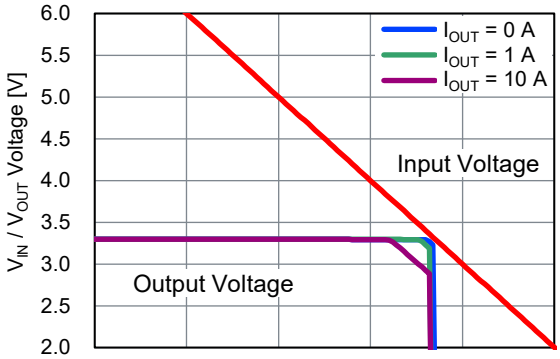
V_{OUT} = 3.3 V, F_{OSC} = 1000 kHz, MODE = “High”
V_{IN} = 0 V to 16 V to 0 V



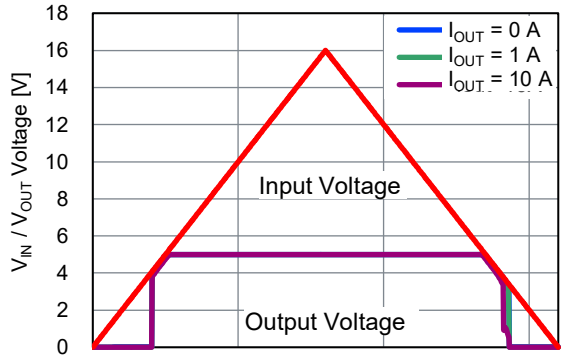
UVLO Release Voltage Zoom-in View



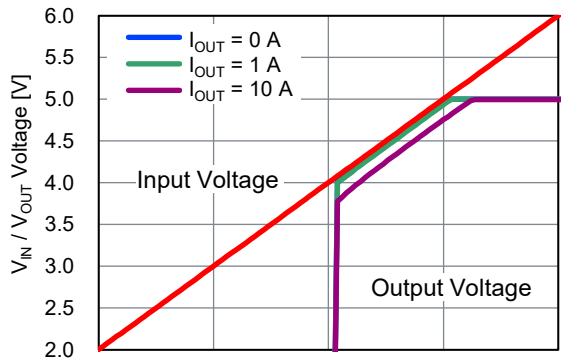
UVLO Detection Voltage Zoom-in View



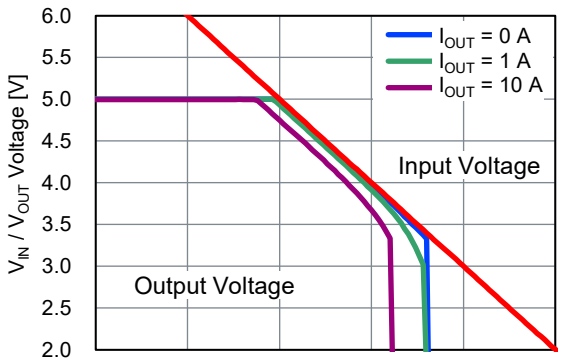
V_{OUT} = 5 V, F_{OSC} = 250 kHz, MODE = “High”
V_{IN} = 0 V to 16 V to 0 V



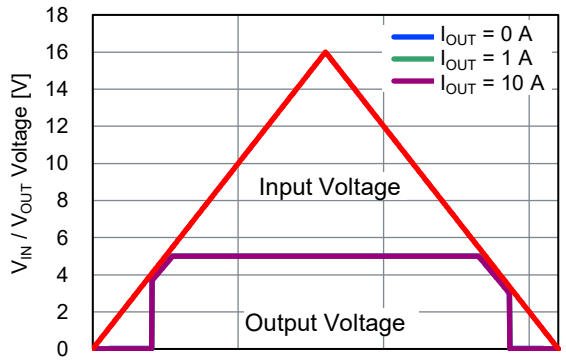
UVLO Release Voltage Zoom-in View



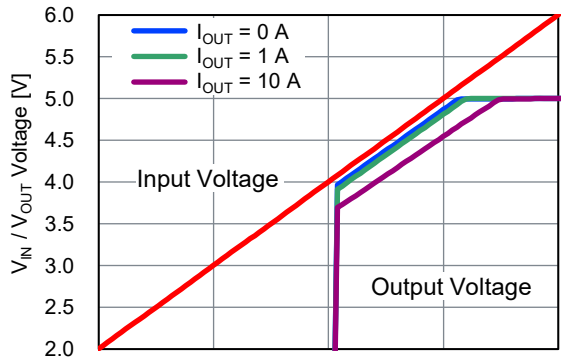
UVLO Detection Voltage Zoom-in View



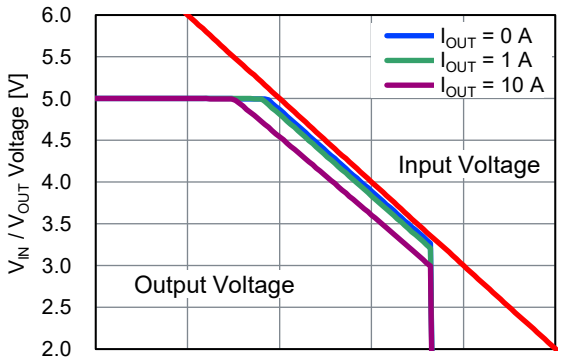
V_{OUT} = 5 V, F_{OSC} = 1000 kHz, MODE = “High”
V_{IN} = 0 V to 16 V to 0 V



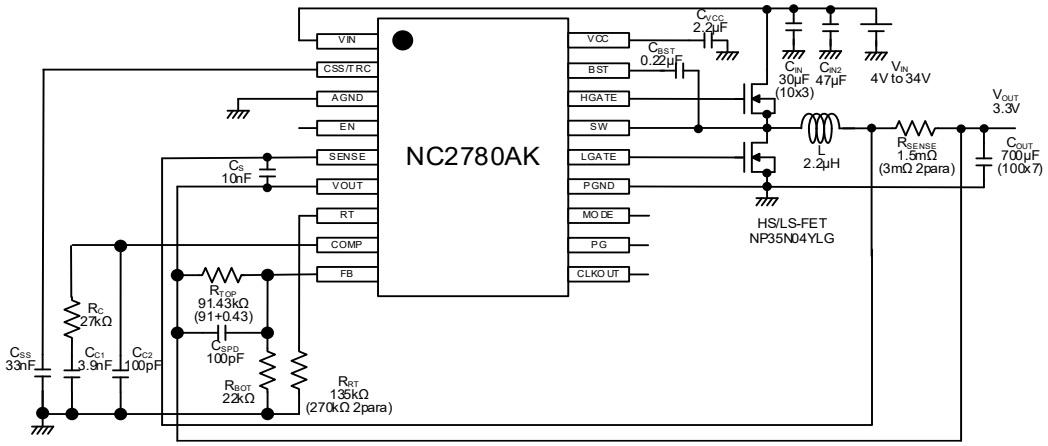
UVLO Release Voltage Zoom-in View



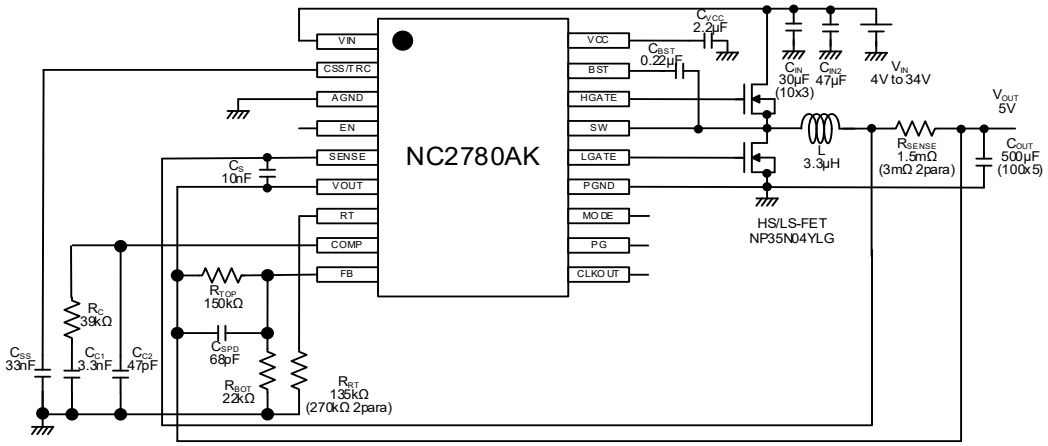
UVLO Detection Voltage Zoom-in View



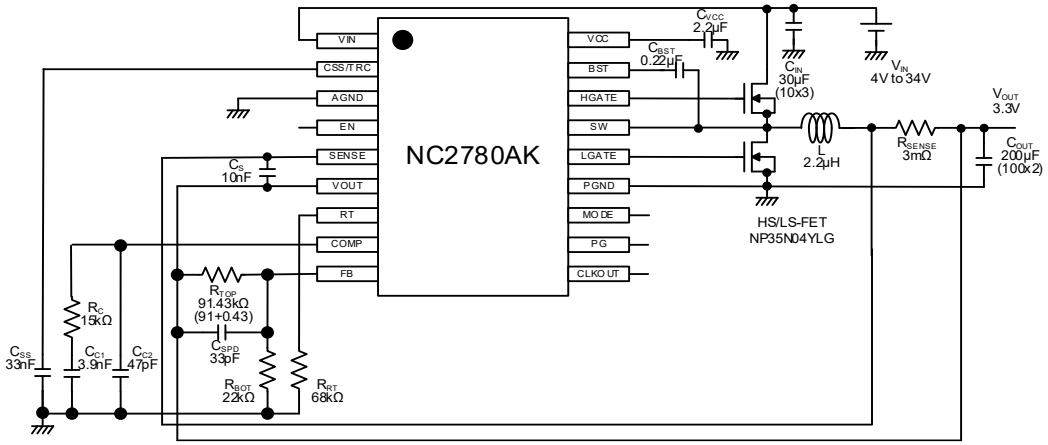
TEST CIRCUIT



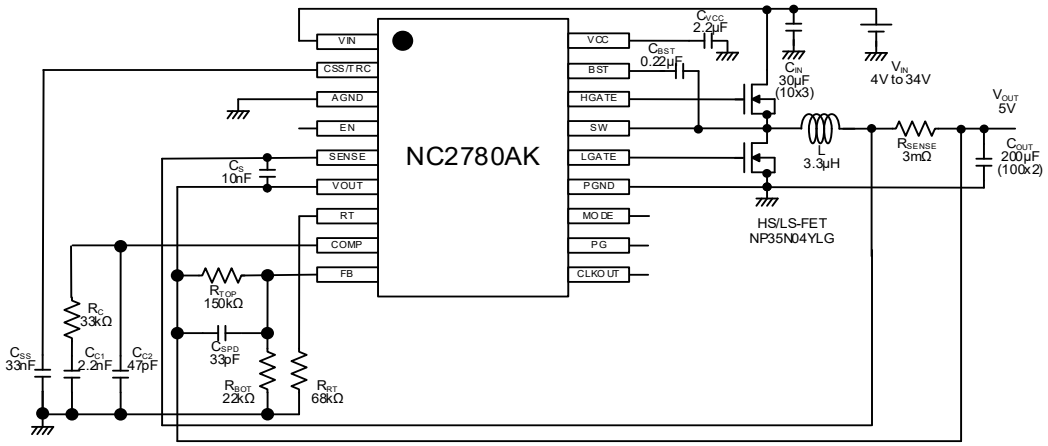
NC2780 Test Circuit (3.3 V / 250 kHz)



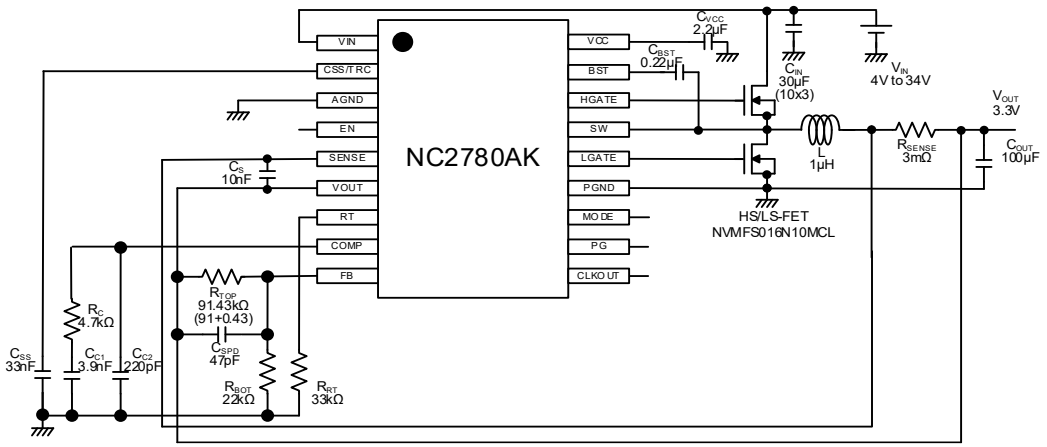
NC2780 Test Circuit (5 V / 250 kHz)



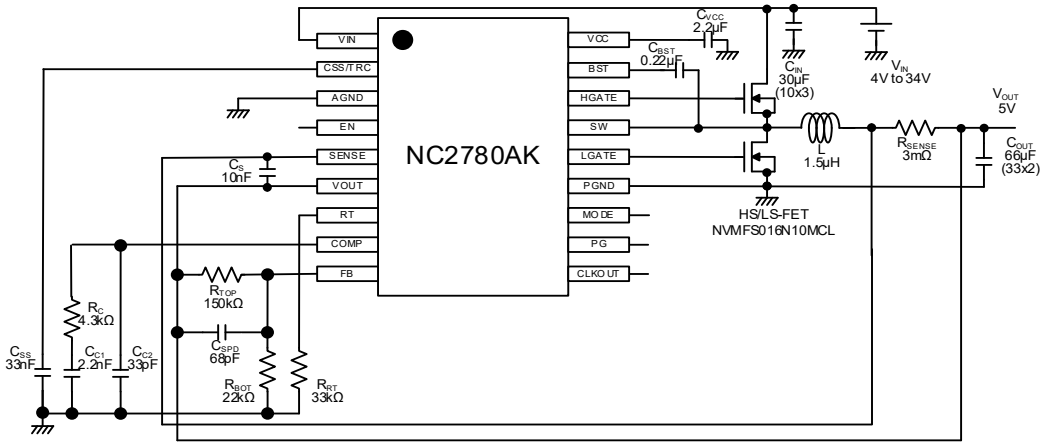
NC2780 Test Circuit (3.3 V / 500 kHz)



NC2780 Test Circuit (5 V / 500 kHz)



NC2780 Test Circuit (3.3 V / 1 MHz)



NC2780 Test Circuit (5 V / 1 MHz)

【Components list for our evaluation】

Symbol	Specs	Manufacturer	Parts Number
C_{IN}	10 µF, 50 V, 125°C	TDK	CGA6P3X7S1H106K
	47 µF, 63 V, 105°C	Nichicon	PLV1J470MDL1TD
C_{BST}	0.22 µF, 25 V, 125°C	Murata	GCM188R71E224KA55D
C_{VCC}	2.2 µF, 25 V, 125°C	Murata	GCM21BR71E225KA73L
C_{OUT}	33 µF, 16 V, 125°C	TDK	CGA8P1X7R1C336M
	100 µF, 16 V, 125°C	TDK	CKG57NX7S1C107M
L	1.0 µH, 5.60mΩ, 13.3 A	TDK	SPM6545VT-1R0M-D
	1.5 µH, 7.40mΩ, 11.6 A	TDK	SPM6545VT-1R5M-D
	2.2 µH, 7.40mΩ, 12.0 A	TDK	SPM7054VT-2R2M-D
	2.2 µH, 2.62mΩ, 18.5 A	SAGAMI ELEC	XRK1365B-2R2M
	3.3 µH, 4.90mΩ, 16.8 A	TDK	SPM12565VT-3R3M-D
	3.3 µH, 3.55mΩ, 16.5 A	SAGAMI ELEC	XRK1365B-3R3M
R_{SENSE}	3mΩ, 1%, 3W	Bourns	CRE2512-FZ-R003E-3

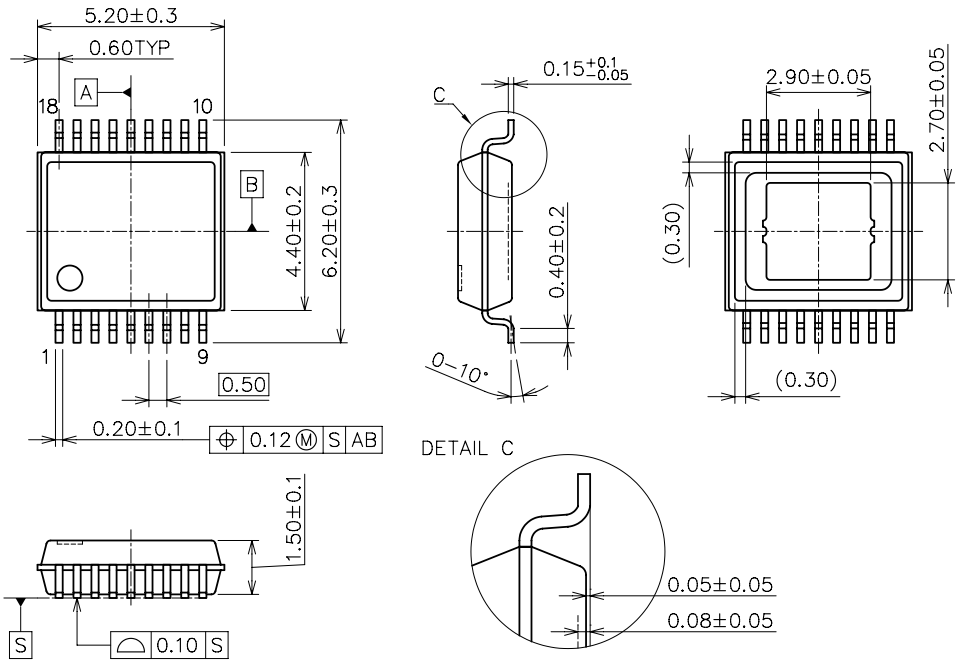
Nisshinbo Micro Devices Inc.

HSOP-18-AK

PI-HSOP-18-AK-E-B

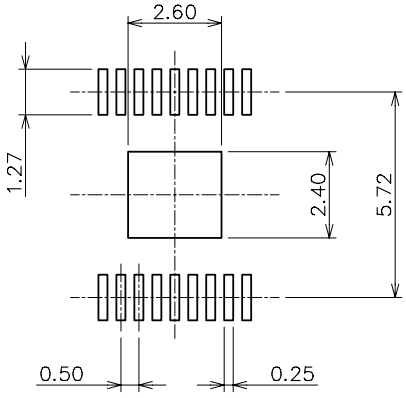
■ PACKAGE DIMENSIONS

UNIT: mm



■ EXAMPLE OF SOLDER PADS DIMENSIONS

UNIT: mm



<Instructions for mounting>

Please be careful when mounting, because there is a standoff on the backside electrode of the package.

Nisshinbo Micro Devices Inc.

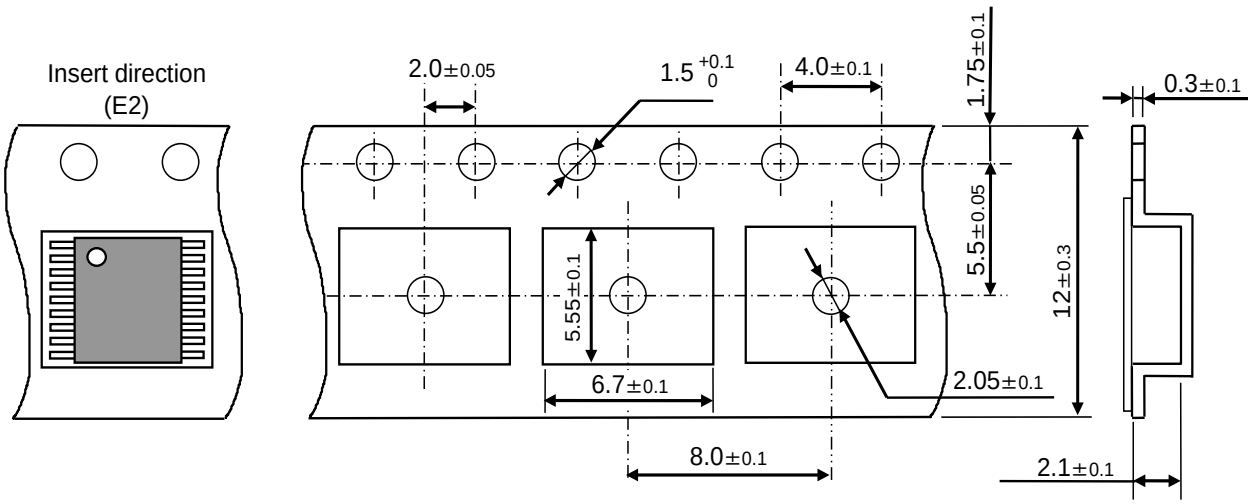
HSOP-18-AK

PI-HSOP-18-AK-E-B

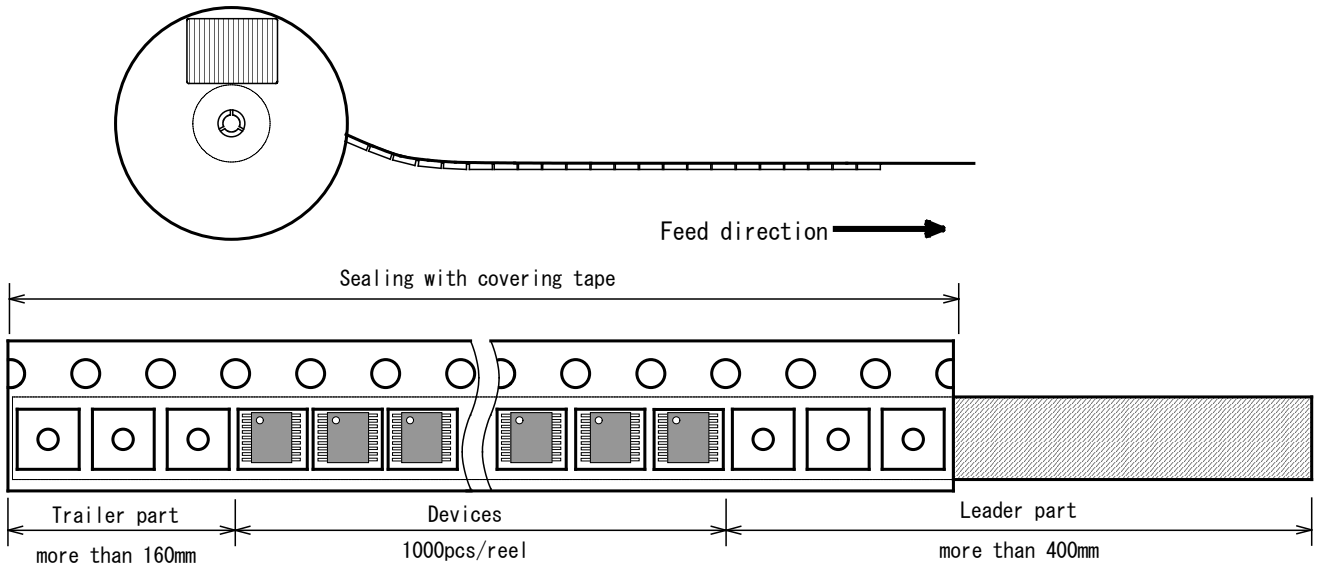
■ **PACKING SPEC**

UNIT: mm

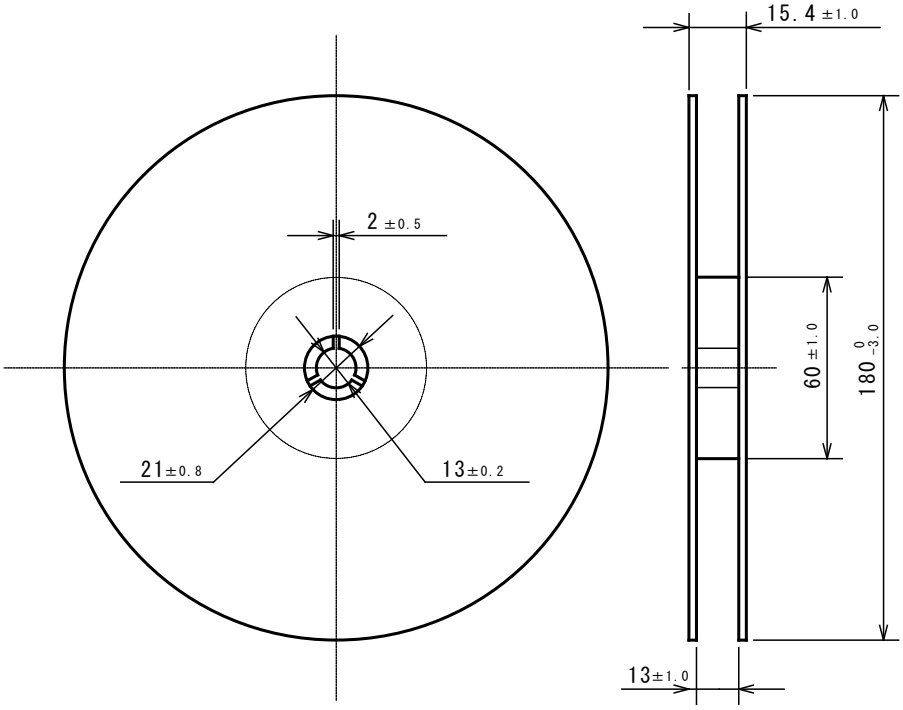
(1) Taping dimensions / Insert direction



(2) Taping state

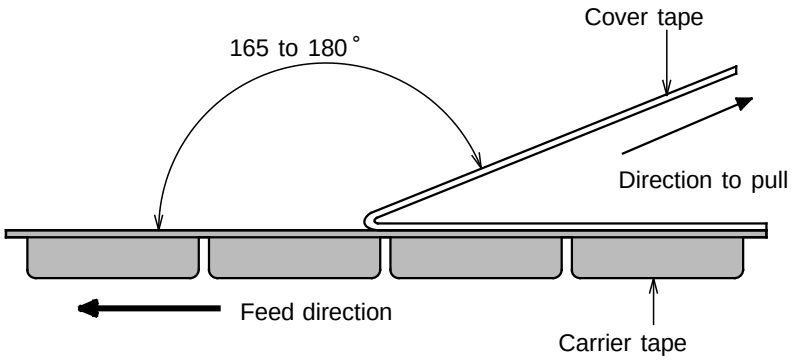


(3) Reel dimensions

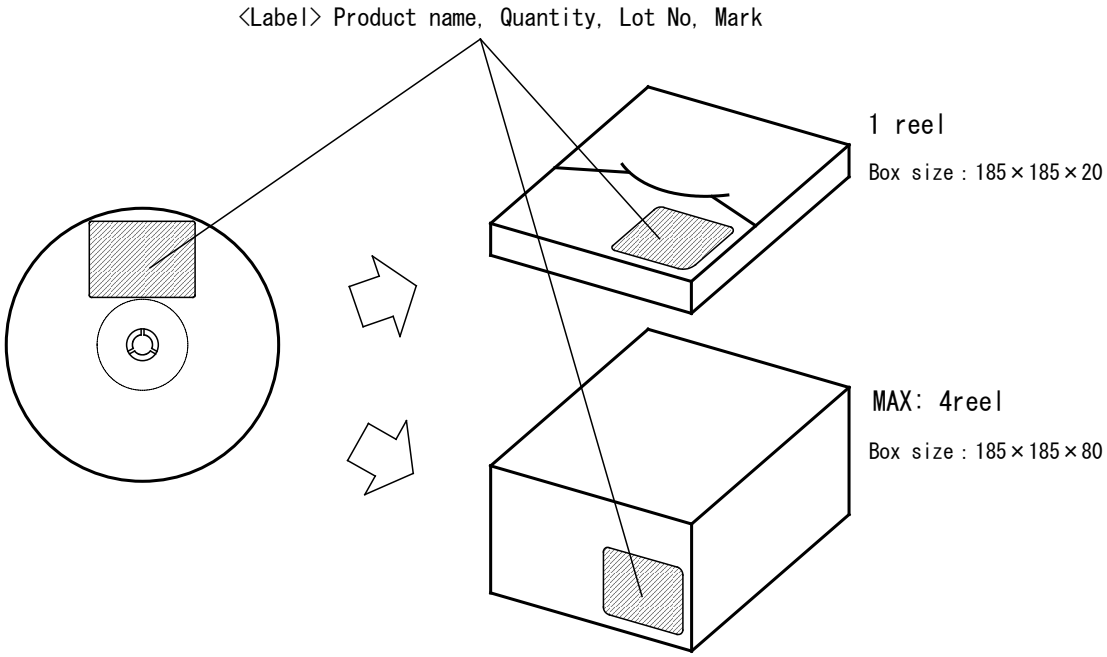


(4) Peeling strength

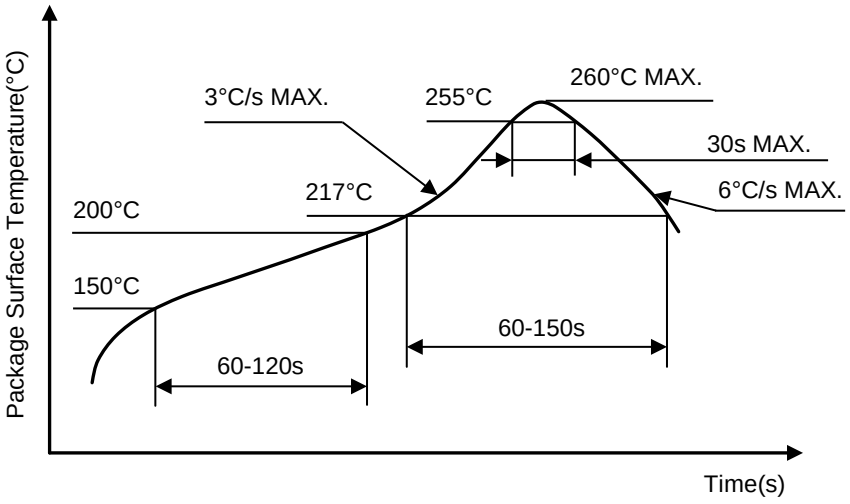
Peeling strength of cover tape
- Peeling angle 165 to 180° degrees to the taped surface.
- Peeling speed 300mm/min
- Peeling strength 0.1 to 1.3N



(5) Packing state



■ **HEAT-RESISTANCE PROFILES**



Reflow profile

Revision History

Date	Revision	Changes
Nov.10.2023	1.0	Initial release
Feb.02.2024	1.1	Updated “HSOP-18-AK Package Information” to the latest version. (PI-HSOP-18-AK-E-A → PI-HSOP-18-AK-E-B)
June.04.2024	1.2	THERMAL CHARACTERISTICS : Format was changed. (The specification is no change.)

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    - Aerospace Equipment
    - Equipment Used in the Deep Sea
    - Power Generator Control Equipment (nuclear, steam, hydraulic, etc.)
    - Life Maintenance Medical Equipment
    - Fire Alarms / Intruder Detectors
    - Vehicle Control Equipment (automotive, airplane, railroad, ship, etc.)
    - Various Safety Devices
    - Traffic control system
    - Combustion equipment

    In case your company desires to use this product for any applications other than general electronic equipment mentioned above, make sure to contact our company in advance. Note that the important requirements mentioned in this section are not applicable to cases where operation requirements such as application conditions are confirmed by our company in writing after consultation with your company.
6. We are making our continuous effort to improve the quality and reliability of our products, but semiconductor products are likely to fail with certain probability. In order to prevent any injury to persons or damages to property resulting from such failure, customers should be careful enough to incorporate safety measures in their design, such as redundancy feature, fire containment feature and fail-safe feature. We do not assume any liability or responsibility for any loss or damage arising from misuse or inappropriate use of the products.
7. The products have been designed and tested to function within controlled environmental conditions. Do not use products under conditions that deviate from methods or applications specified in this datasheet. Failure to employ the products in the proper applications can lead to deterioration, destruction or failure of the products. We shall not be responsible for any bodily injury, fires or accident, property damage or any consequential damages resulting from misuse or misapplication of the products.
8. Quality Warranty
    8-1. Quality Warranty Period
    In the case of a product purchased through an authorized distributor or directly from us, the warranty period for this product shall be one (1) year after delivery to your company. For defective products that occurred during this period, we will take the quality warranty measures described in section 8-2. However, if there is an agreement on the warranty period in the basic transaction agreement, quality assurance agreement, delivery specifications, etc., it shall be followed.
    8-2. Quality Warranty Remedies
    When it has been proved defective due to manufacturing factors as a result of defect analysis by us, we will either deliver a substitute for the defective product or refund the purchase price of the defective product.
    Note that such delivery or refund is sole and exclusive remedies to your company for the defective product.
    8-3. Remedies after Quality Warranty Period
    With respect to any defect of this product found after the quality warranty period, the defect will be analyzed by us. On the basis of the defect analysis results, the scope and amounts of damage shall be determined by mutual agreement of both parties. Then we will deal with upper limit in Section 8-2. This provision is not intended to limit any legal rights of your company.
9. Anti-radiation design is not implemented in the products described in this document.
10. The X-ray exposure can influence functions and characteristics of the products. Confirm the product functions and characteristics in the evaluation stage.
11. WLCSP products should be used in light shielded environments. The light exposure can influence functions and characteristics of the products under operation or storage.
12. Warning for handling Gallium and Arsenic (GaAs) products (Applying to GaAs MMIC, Photo Reflector). These products use Gallium (Ga) and Arsenic (As) which are specified as poisonous chemicals by law. For the prevention of a hazard, do not burn, destroy, or process chemically to make them as gas or power. When the product is disposed of, please follow the related regulation and do not mix this with general industrial waste or household waste.
13. Please contact our sales representatives should you have any questions or comments concerning the products or the technical information.

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Nisshinbo Micro Devices Inc.

Official website

https://www.nisshinbo-microdevices.co.jp/en/

Purchase information

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