



Automotive NT1191GEAE3A GNSS Wideband Low Noise Amplifier

FEATURES

- AEC-Q100 grade 2
- Frequency range: 1164 MHz to 1610 MHz
- Supply voltage: 1.5 V to 5.5 V (3.3 V typ.)
- Current consumption: 5.5 mA typ.
- Gain: 17.5 dB typ. @ L1/L2/L5/L6 band
- NF: 0.75 dB typ. @ L1/L2/L5/L6 band
- P-1dB(IN): -10 dBm typ. @ L1/L2/L5/L6 band
- IIP3: 0 dBm typ. @ L1/L2/L5/L6 band
- With stand-by function
- Package size: 1.6 x 1.6 mm typ.
t = 0.83 mm max.
- Operating temperature range: -40 to +105°C
- RoHS compliant and Halogen Free, MSL1

APPLICATIONS

- GNSS (GPS, GLONASS, Galileo, BeiDou, etc.) receiver application for automotive
- Multi-GNSS application for high-precision positioning
- GNSS module for automotive
- Active antenna, car navigation, dashboard camera, GNSS tracker

GENERAL DESCRIPTION

The NT1191GEAE3A is a GNSS wideband low noise amplifier (LNA) intended for automotive multi-GNSS receiver applications.

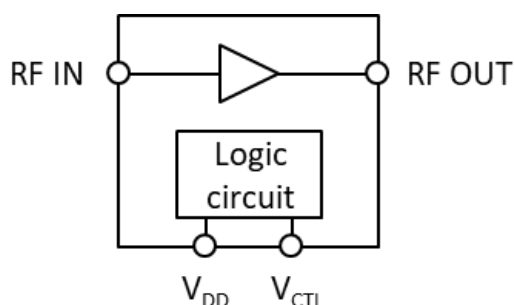
The NT1191GEAE3A features good gain flatness and low noise figure (NF) in the entire GNSS band from 1164 MHz to 1610 MHz. It supports a high supply voltage up to 5.5 V. Integrated ESD protection device on each port brings excellent ESD robustness. This LNA can operate in wide temperature range from -40 to +105°C.

The DFN package with wettable flank allows to adopt automated optical inspection (AOI) of solder joints, which is especially demanded in automotive applications.



DFN1616-6-GE
1.6 × 1.6 × 0.83 (mm)

BLOCK DIAGRAM



■ PRODUCT NAME INFORMATION

NT1191 GE A E3 A

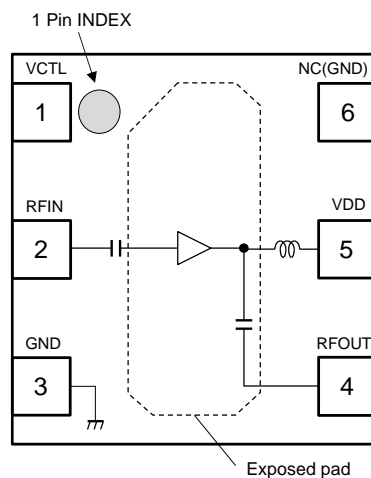
Description of configuration

Suffix	Item	Description
GE	Package code	Indicates the package. Refer to the order information.
A	Version	Indicates the product version. "A" is initial version.
E3	Packing	Refer to the packing specifications.
A	Grade	Indicates the quality grade. "A" means Automotive application. Operating temperature range: -40°C to +105°C, Test temperature: +25°C, +105°C

■ ORDER INFORMATION

PRODUCT NAME	PACKAGE	RoHS	HALOGEN-FREE	PLATING COMPOSITION	WEIGHT (mg)	QUANTITY (pcs/reel)
NT1191GEAE3A	DFN1616-6-GE	Yes	Yes	SnBi	5.4	3000

■ PIN DESCRIPTIONS



DFN1616-6-GE Pin Configuration

Pin No.	Pin Name	Description
1	VCTL	Control signal input terminal
2	RFIN	RF input terminal
3	GND	Ground terminal
4	RFOUT	RF output terminal
5	VDD	Operating voltage supply terminal
6	NC(GND)	No connected terminal (connect to ground)
-	Exposed pad	Ground terminal

Please refer to "[APPLICATION CIRCUIT](#)" for details.

■ TRUTH TABLE

"H"= $V_{CTL}(H)$, "L"= $V_{CTL}(L)$

V_{CTL}	Mode
H	Active mode
L	Stand-by mode

■ ABSOLUTE MAXIMUM RATINGS

General conditions: $T_a = +25^{\circ}\text{C}$, $Z_s = Z_l = 50\Omega$

	Symbol	Ratings	Unit
Supply Voltage	V_{DD}	6.0	V
Control Voltage	V_{CTL}	6.0	V
Input Power	P_{IN}^{*1}	+15	dBm
Power Dissipation	P_D^{*2}	1100	mW
Operating Temperature Range	T_{opr}	-40 to +105	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	-55 to +150	$^{\circ}\text{C}$

^{*1} $V_{DD} = 3.3\text{ V}$ ^{*2} 4-layer FR4 PCB with through-hole (101.5 x 114.5 mm), $T_j = 150^{\circ}\text{C}$,

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

Calculate the power consumption of the IC from the operating conditions and calculate the junction temperature with the thermal resistance.

Please refer to "[THERMAL CHARACTERISTICS](#)" for the thermal resistance under our measurement board conditions.

■ THERMAL CHARACTERISTICS

Parameter	Value
Thermal Resistance (θ_{ja})	$\theta_{ja} = 116^{\circ}\text{C/W}$
Thermal Characterization Parameter (ψ_{jt})	$\psi_{jt} = 43^{\circ}\text{C/W}$

 θ_{ja} : Junction-to-Ambient Thermal Resistance ψ_{jt} : Junction-to-Top Thermal Characterization Parameter

■ ELECTROSTATIC DISCHARGE (ESD) PROTECTION VOLTAGE

	Conditions	Pin No.	Pin Name	Protection Voltage		
				Ground	VDD	I/O
HBM	$C = 100\text{ pF}$, $R = 1.5\text{ k}\Omega$	1	VCTL	$\pm 2000\text{ V}$	$\pm 2000\text{ V}$	$\pm 2000\text{ V}$
		2	RFIN	$\pm 2000\text{ V}$	$\pm 1000\text{ V}$	$\pm 2000\text{ V}$
		3	GND	COM.	$\pm 2000\text{ V}$	-
		4	RFOUT	$\pm 2000\text{ V}$	$\pm 2000\text{ V}$	$\pm 2000\text{ V}$
		5	VDD	$\pm 2000\text{ V}$	COM.	-
		6	NC(GND)	-	-	-

	Conditions	Protection Voltage
CDM	Field Induced CDM	$\pm 1000\text{ V}$

ESD PROTECTION VOLTAGE

The electrostatic discharge tests are done based on JEDEC JS-001 and JS-002.

■ RECOMMENDED OPERATING CONDITIONS

	Symbol	Value	Unit
Supply Voltage	V_{DD}	1.5 to 5.5	V
Control Voltage	V_{CTL}	1.5 to 5.5	V
Operating Temperature Range	T_a	-40 to +105	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

■ ELECTRICAL CHARACTERISTICS 1 (DC)

General conditions: $T_a = +25^{\circ}\text{C}$, $Z_s = Z_l = 50\Omega$

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Supply Voltage	V_{DD}		1.5	3.3	5.5	V
Control Voltage (High)	$V_{CTL(H)}$		1.5	1.8	5.5	V
Control Voltage (Low)	$V_{CTL(L)}$		0	0	0.3	V
Operating Current	I_{DD}	RF OFF, $V_{DD} = 3.3\text{ V}$, $V_{CTL} = 1.8\text{ V}$	-	5.5	8.0	mA
		RF OFF, $V_{DD} = 3.3\text{ V}$, $V_{CTL} = 0\text{ V}$	-	0.1	3.0	μA
Control Current	I_{CTL}	RF OFF, $V_{CTL} = 1.8\text{ V}$	-	5	20	μA

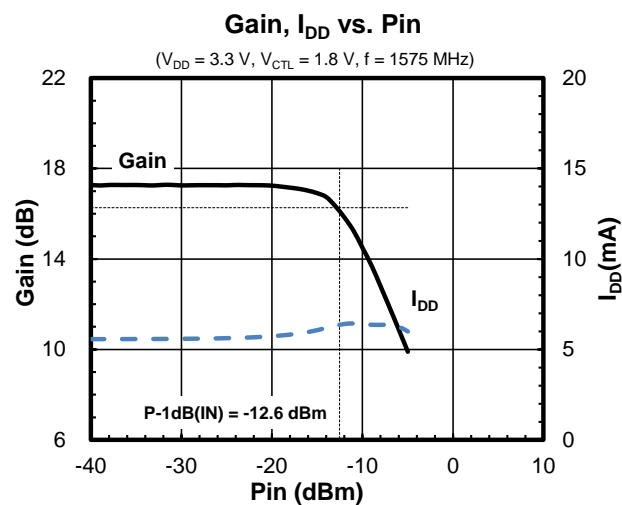
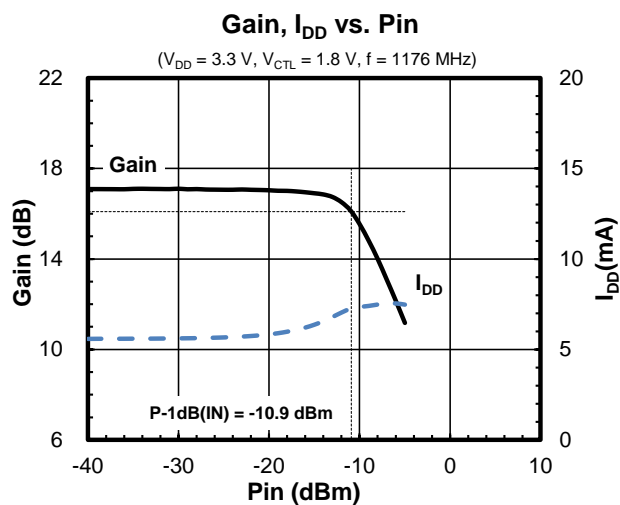
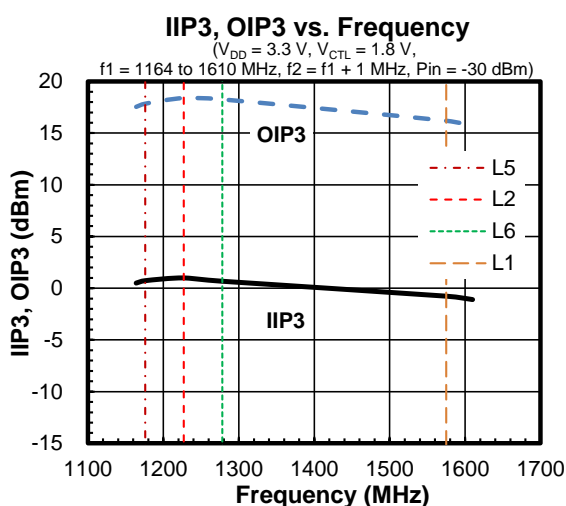
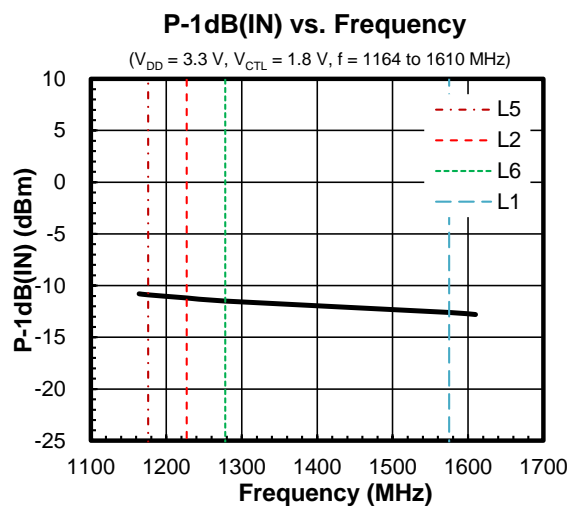
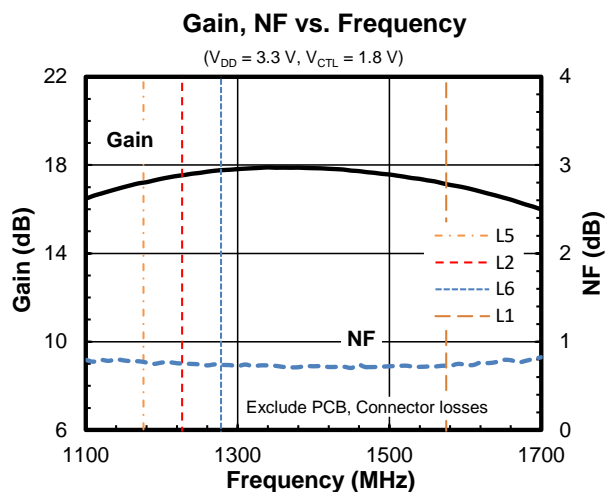
■ ELECTRICAL CHARACTERISTICS 2 (RF)

General conditions: $V_{DD} = 3.3\text{ V}$, $V_{CTL} = 1.8\text{ V}$, $f = 1164\text{ MHz}$ to 1610 MHz , $T_a = +25^\circ\text{C}$, $Z_s = Z_l = 50\Omega$, with application circuit

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Small Signal Gain	Gain	$f = 1176\text{ MHz}$ (L5 band), Exclude PCB, connector loss (0.09 dB)	15.0	17.5	19.0	dB
		$f = 1227\text{ MHz}$ (L2 band), Exclude PCB, connector loss (0.10 dB)				
		$f = 1278\text{ MHz}$ (L6 band), Exclude PCB, connector loss (0.11 dB)				
		$f = 1575\text{ MHz}$ (L1 band), Exclude PCB, connector loss (0.14 dB)				
Noise Figure	NF	$f = 1176\text{ MHz}$ (L5 band), Exclude PCB, connector loss (0.04 dB)	-	0.75	1.10	dB
		$f = 1227\text{ MHz}$ (L2 band), Exclude PCB, connector loss (0.04 dB)				
		$f = 1278\text{ MHz}$ (L6 band), Exclude PCB, connector loss (0.05 dB)				
		$f = 1575\text{ MHz}$ (L1 band), Exclude PCB, connector loss (0.06 dB)				
Isolation	ISL	$f = 1176\text{ MHz}$ (L5 band)	32	35	-	dB
		$f = 1227\text{ MHz}$ (L2 band)				
		$f = 1278\text{ MHz}$ (L6 band)				
		$f = 1575\text{ MHz}$ (L1 band)				
Input Power at 1 dB Gain Compression Point	P-1dB(IN)	$f = 1176\text{ MHz}$ (L5 band)	-15.0	-10.0	-	dBm
		$f = 1227\text{ MHz}$ (L2 band)				
		$f = 1278\text{ MHz}$ (L6 band)				
		$f = 1575\text{ MHz}$ (L1 band)				
Input 3rd Order Intercept Point	IIP3	$f_1 = 1176\text{ MHz}$, $f_2 = f_1 + 1\text{ MHz}$, Pin = -30 dBm	-5.0	0	-	dBm
		$f_1 = 1227\text{ MHz}$, $f_2 = f_1 + 1\text{ MHz}$, Pin = -30 dBm				
		$f_1 = 1278\text{ MHz}$, $f_2 = f_1 + 1\text{ MHz}$, Pin = -30 dBm				
		$f_1 = 1575\text{ MHz}$, $f_2 = f_1 + 1\text{ MHz}$, Pin = -30 dBm				
RF IN Return Loss	RLi	$f = 1176\text{ MHz}$ (L5 band)	6.0	12.0	-	dB
		$f = 1227\text{ MHz}$ (L2 band)				
		$f = 1278\text{ MHz}$ (L6 band)				
		$f = 1575\text{ MHz}$ (L1 band)				
RF OUT Return Loss	RLo	$f = 1176\text{ MHz}$ (L5 band)	10.0	18.0	-	dB
		$f = 1227\text{ MHz}$ (L2 band)				
		$f = 1278\text{ MHz}$ (L6 band)				
		$f = 1575\text{ MHz}$ (L1 band)				

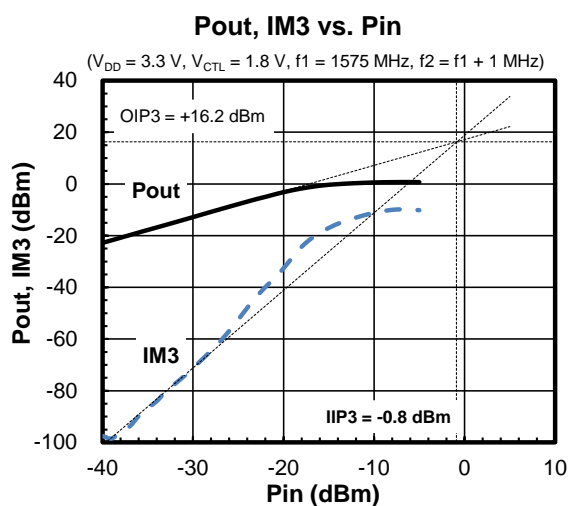
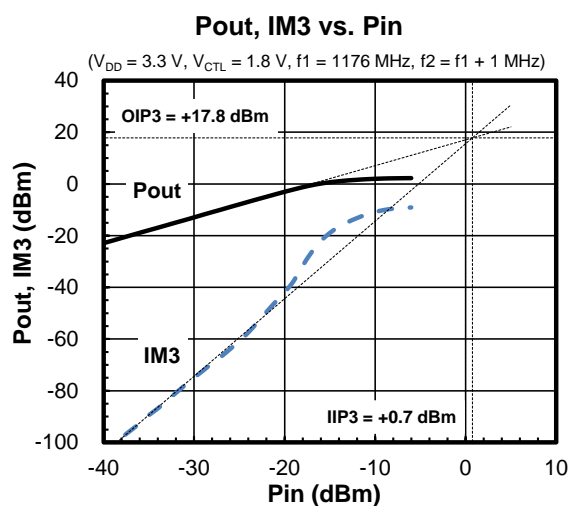
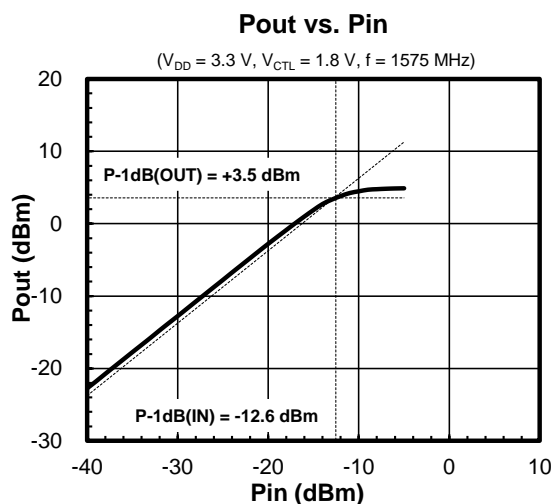
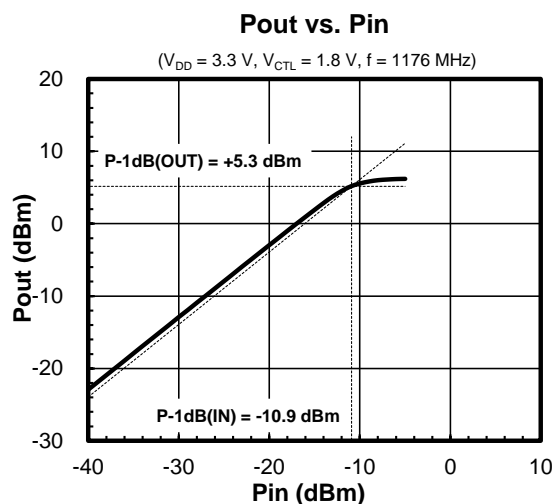
■ TYPICAL CHARACTERISTICS

Conditions: $V_{DD} = 3.3\text{ V}$, $V_{CTL} = 1.8\text{ V}$, $T_a = +25^\circ\text{C}$, $Z_s = Z_L = 50\Omega$, with application circuit
(Typical characteristics are intended to be used as reference data, they are not guaranteed.)



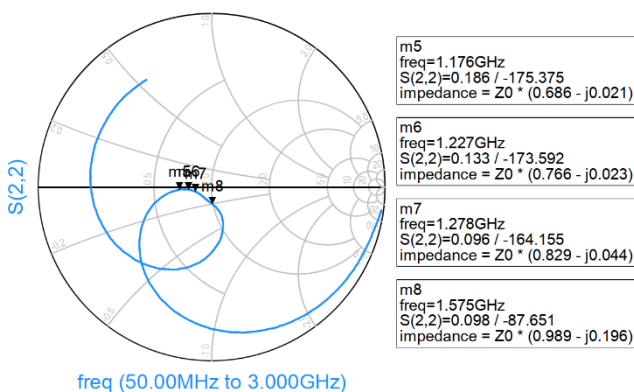
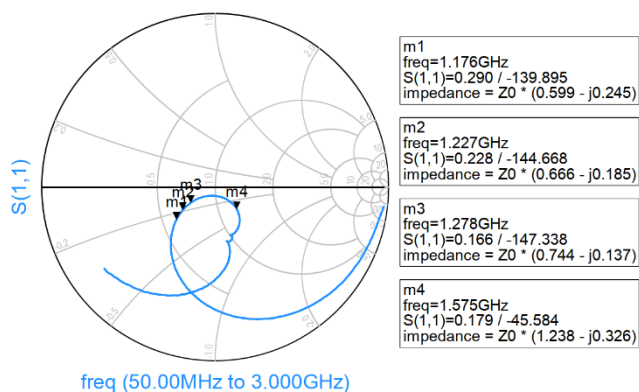
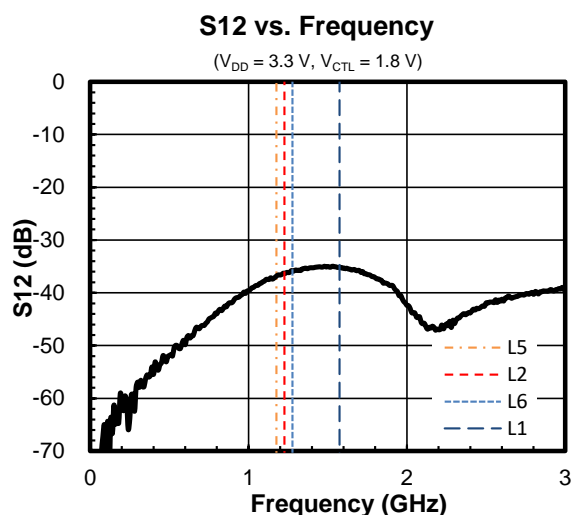
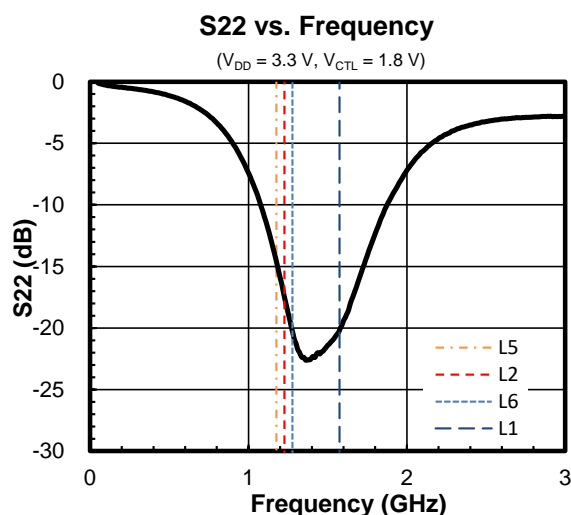
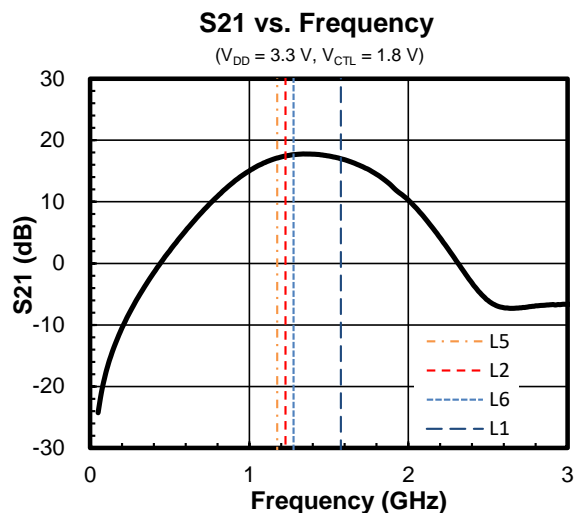
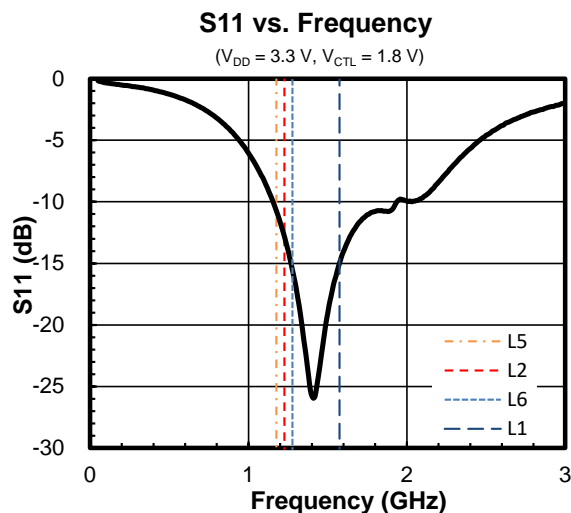
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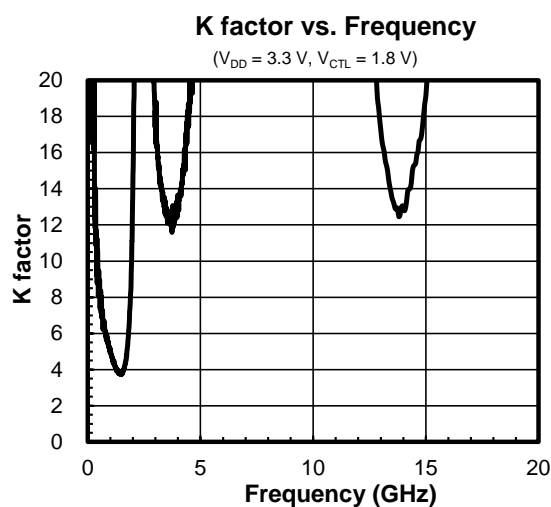
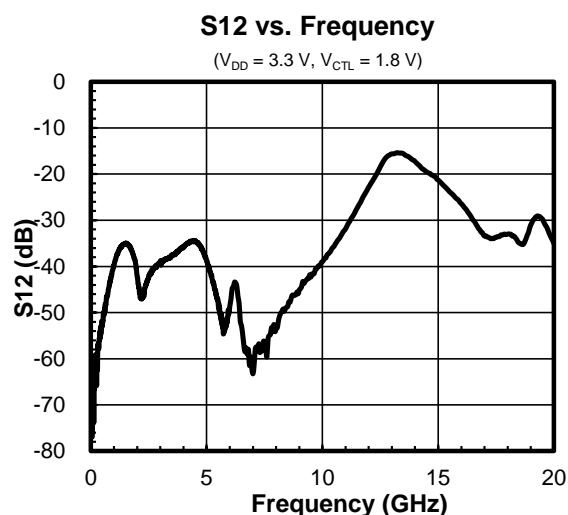
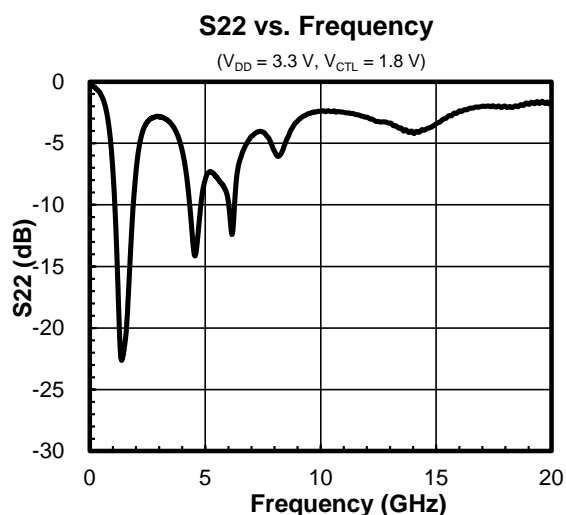
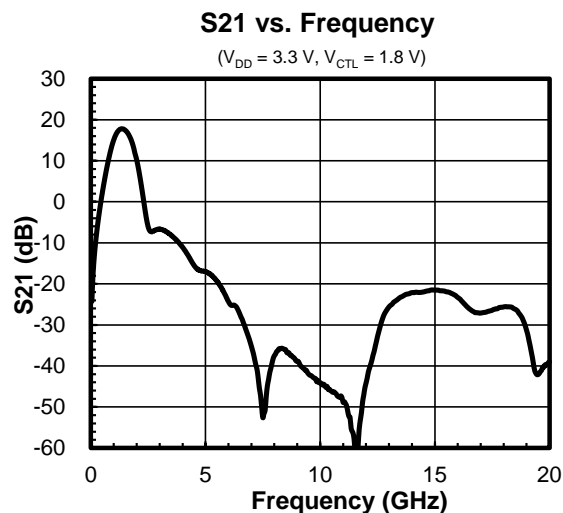
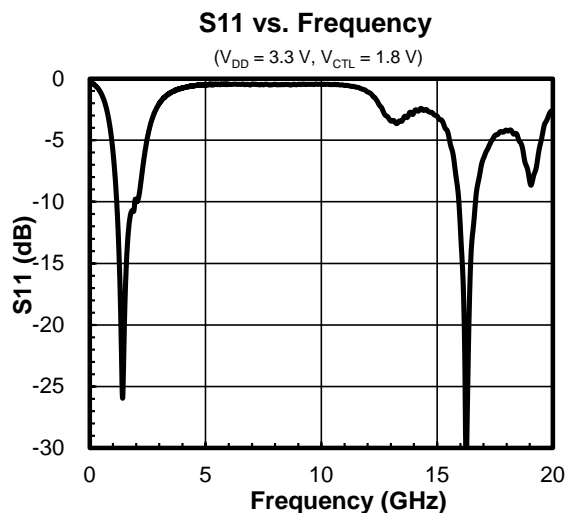
■ TYPICAL CHARACTERISTICS

Conditions: $V_{DD} = 3.3\text{ V}$, $V_{CTL} = 1.8\text{ V}$, $f = 50\text{ MHz to }3\text{ GHz}$, $T_a = +25^\circ\text{C}$, $Z_s = Z_l = 50\Omega$, with application circuit
(Typical characteristics are intended to be used as reference data, they are not guaranteed.)



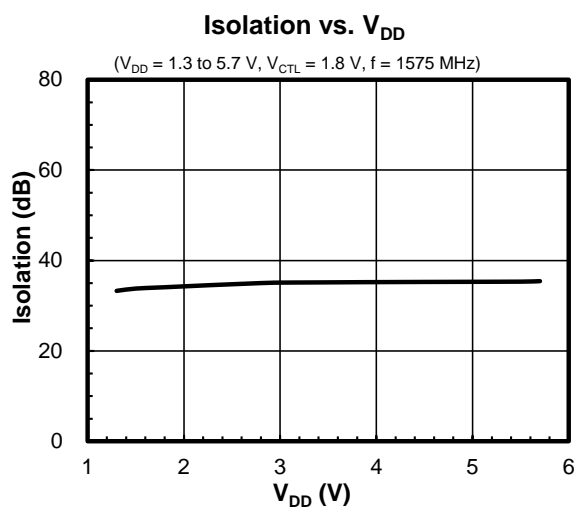
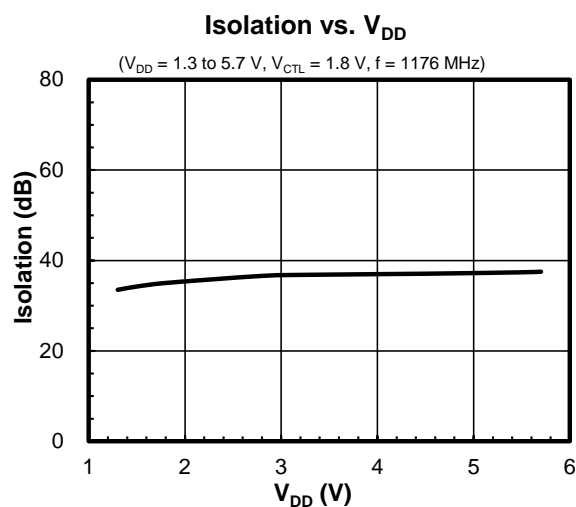
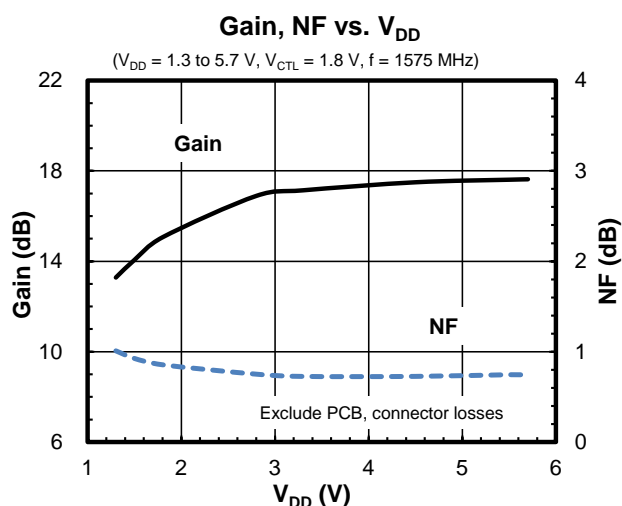
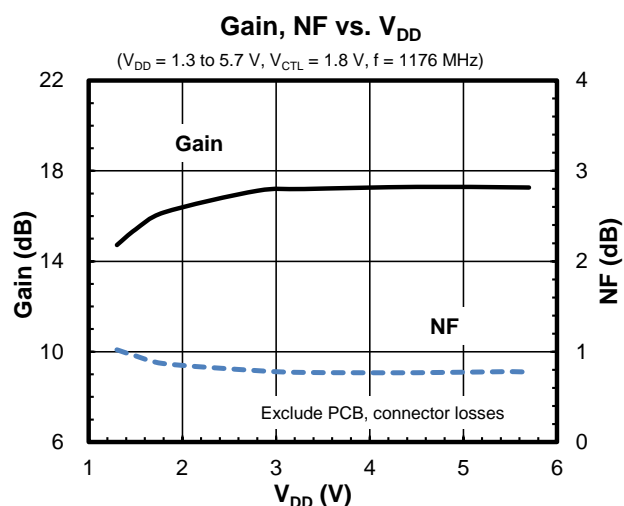
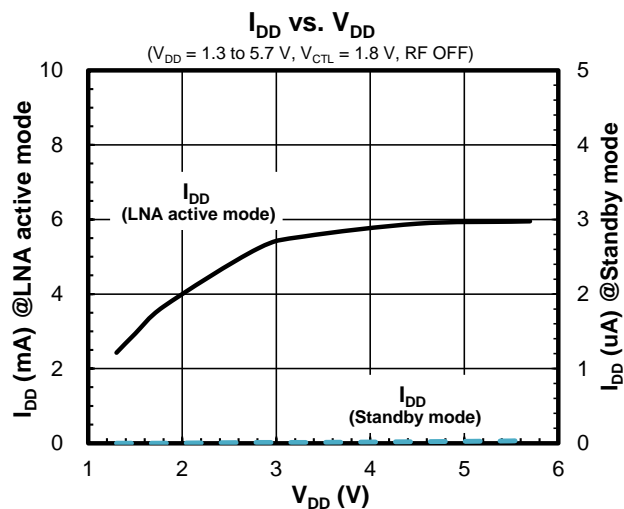
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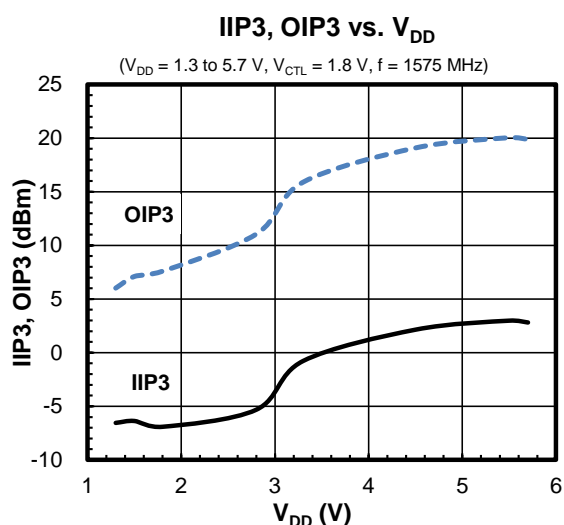
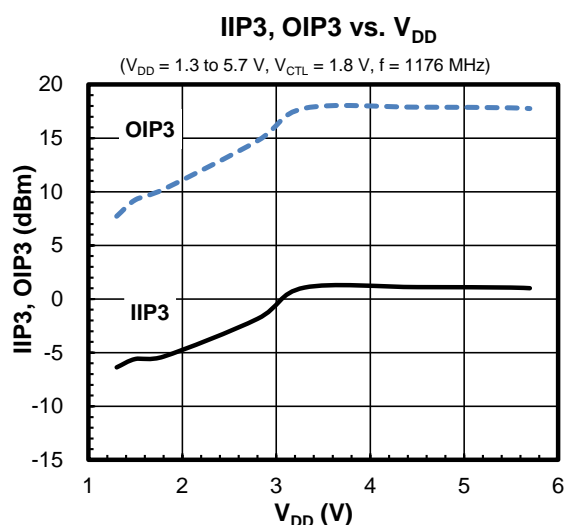
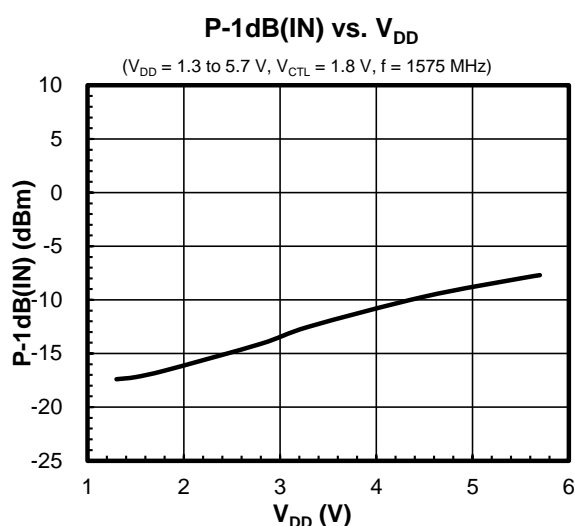
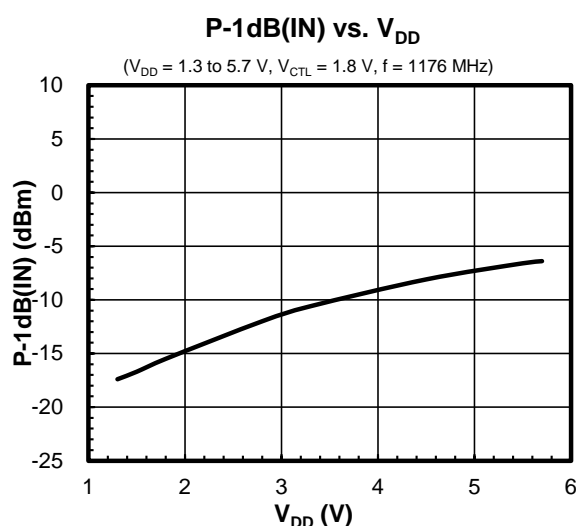
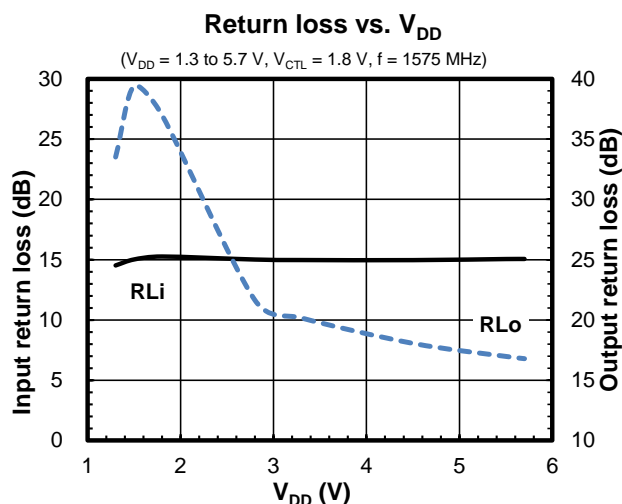
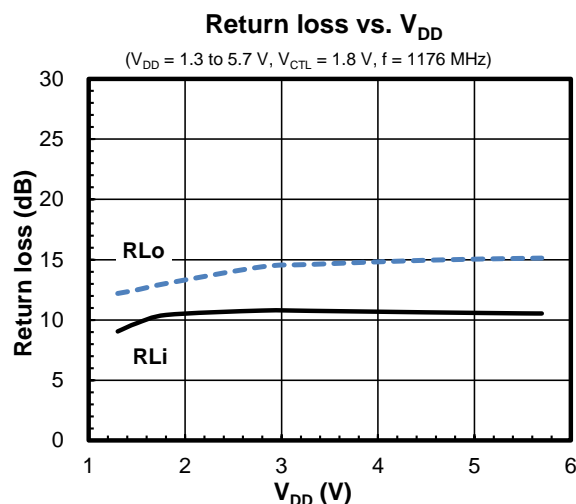
■ TYPICAL CHARACTERISTICS

Conditions: $V_{CTL} = 1.8\text{ V}$, $T_a = +25^\circ\text{C}$, $Z_s = Z_l = 50\Omega$, with application circuit
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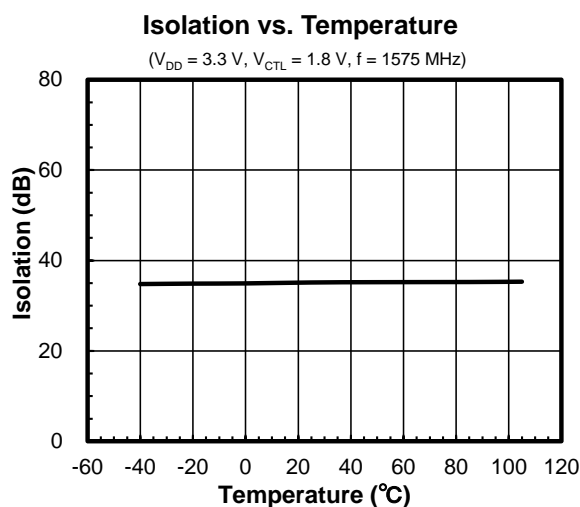
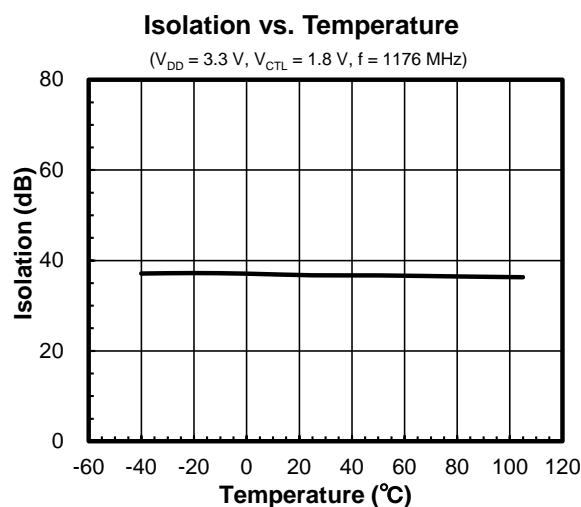
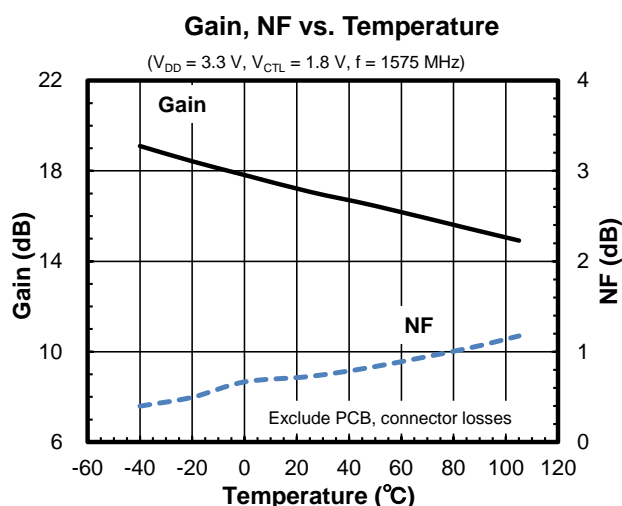
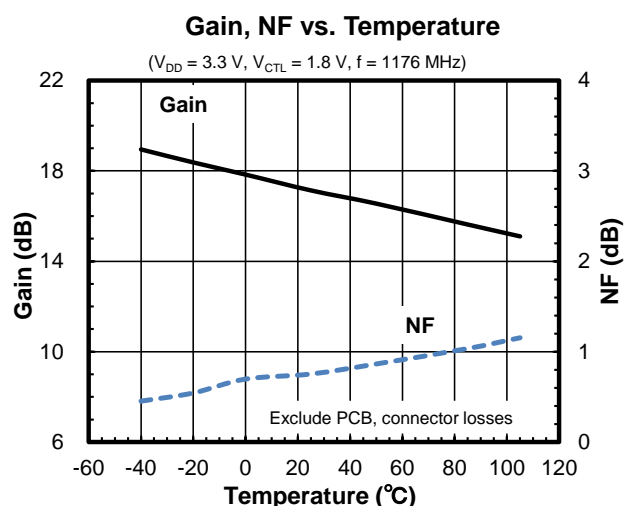
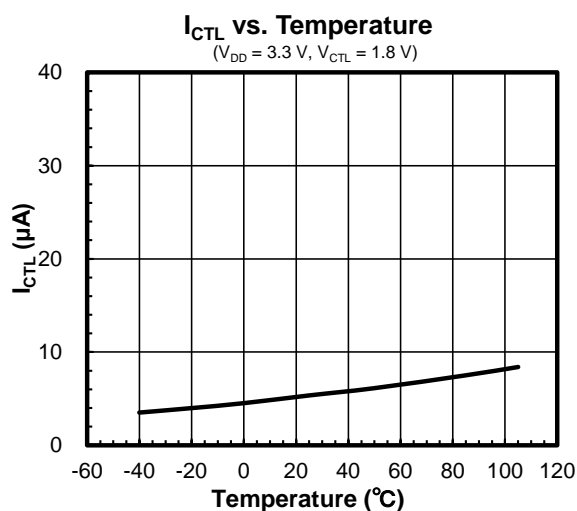
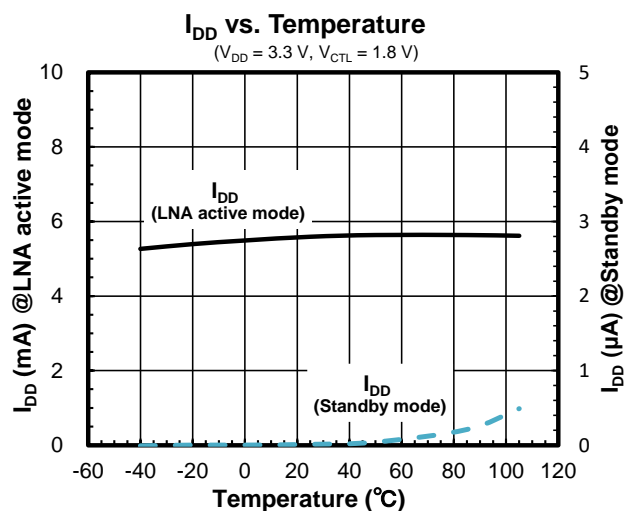
■ TYPICAL CHARACTERISTICS

Conditions: $V_{CTL} = 1.8\text{ V}$, $T_a = +25^\circ\text{C}$, $Z_s = Z_l = 50\Omega$, with application circuit
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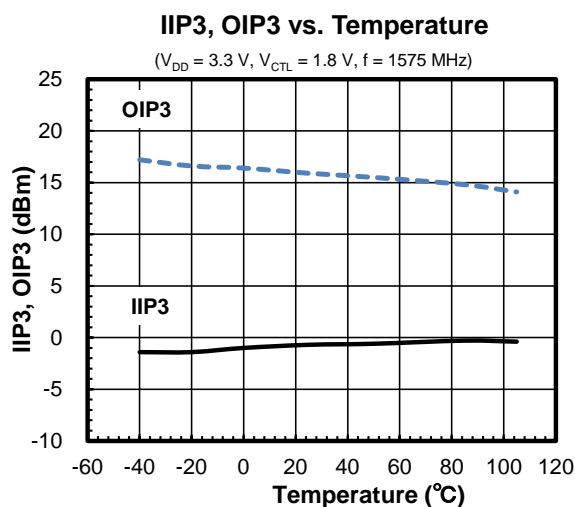
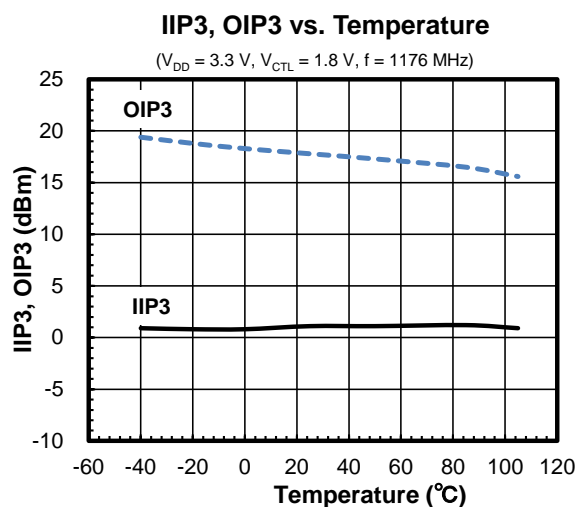
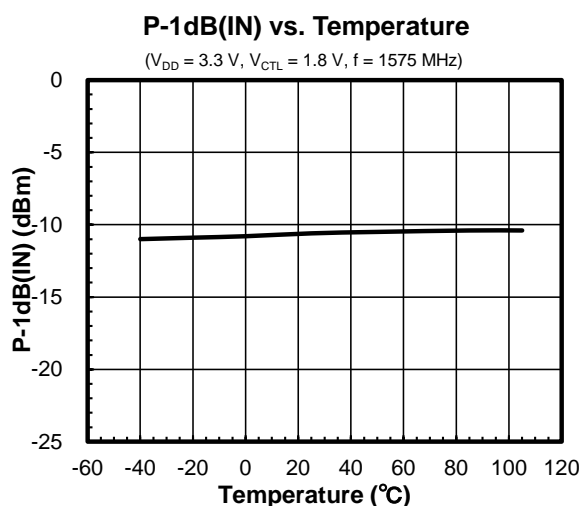
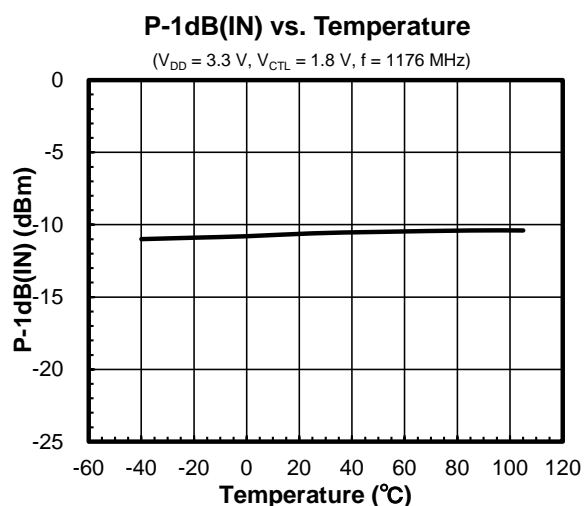
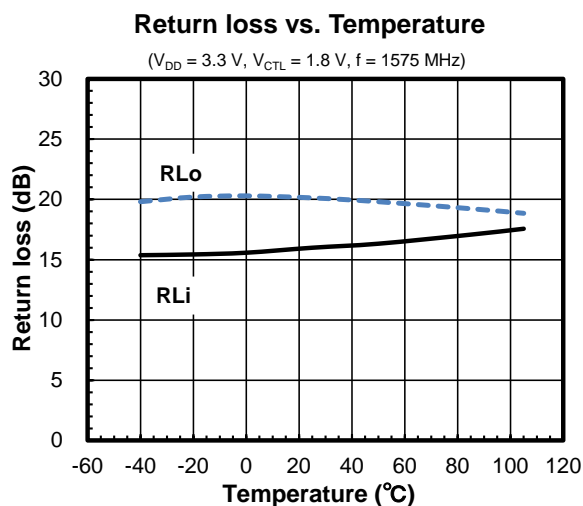
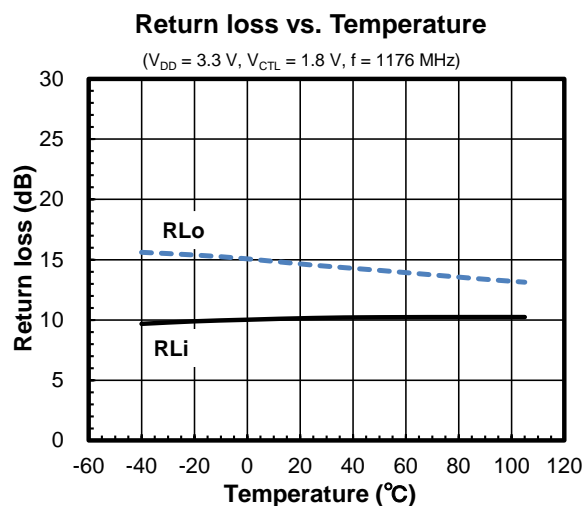
■ TYPICAL CHARACTERISTICS

Conditions: $V_{DD} = 3.3\text{ V}$, $V_{CTL} = 1.8\text{ V}$, $Z_s = Z_l = 50\Omega$, with application circuit
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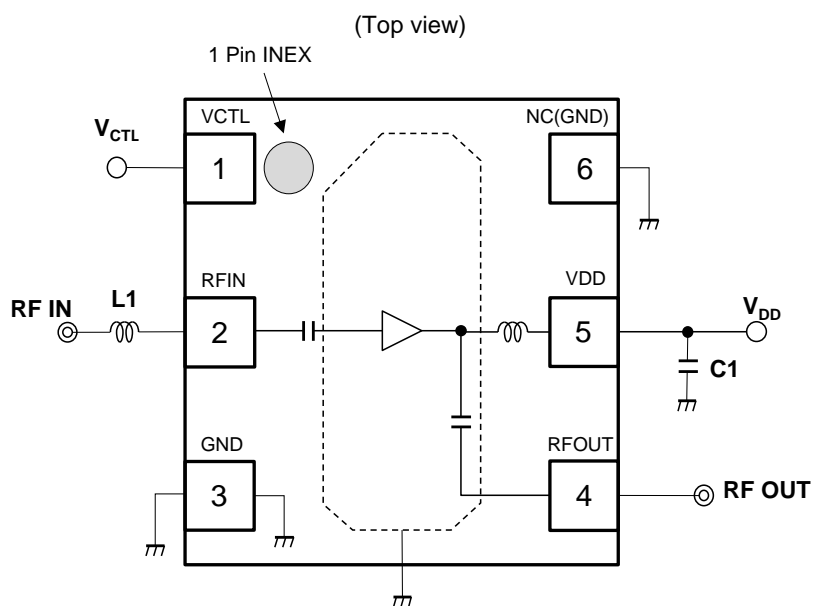


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■ APPLICATION CIRCUIT

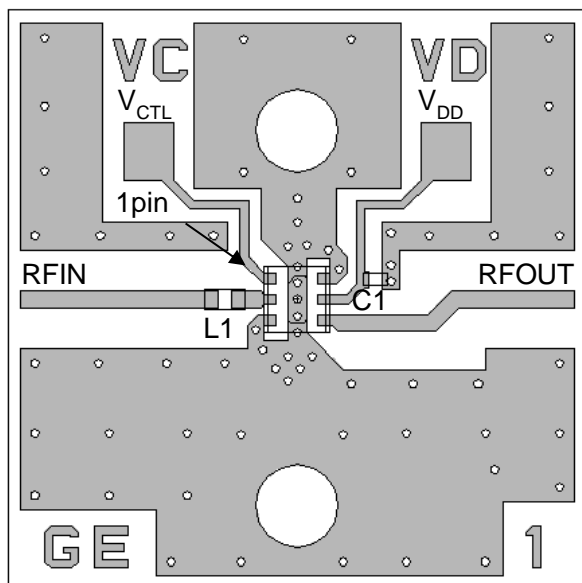


NT1191GEAE3A Typical Application Circuit

<Parts list>

Part ID	Value	Notes
L1	9.5 nH	LQW15AN_00 series (MURATA)
C1	1000 pF	GRM03 series (MURATA)

■ Evaluation Board / PCB layout



PCB

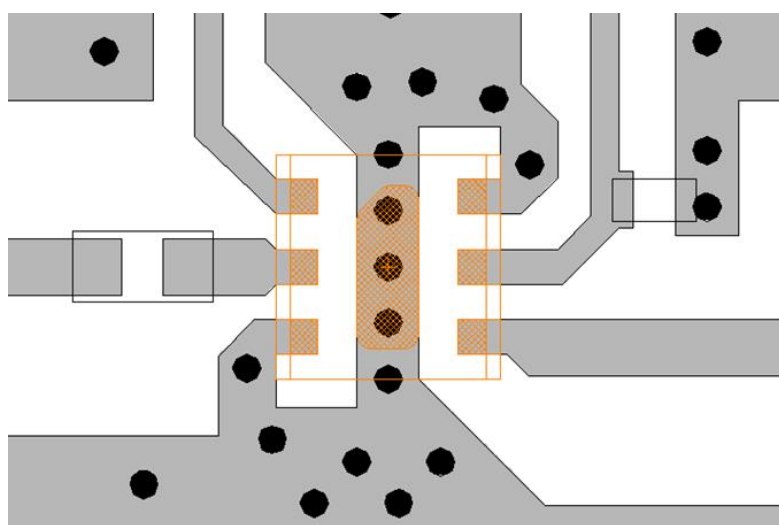
Substrate: FR-4

Thickness: 0.2 mm

Microstrip line width: 0.4 mm ($Z_0 = 50\Omega$)

Size: 14.0 x 14.0 mm

<PCB layout guideline>



PCB

PKG Terminal

PKG Outline

GND Via Hole

Diameter $\phi = 0.2$ mm

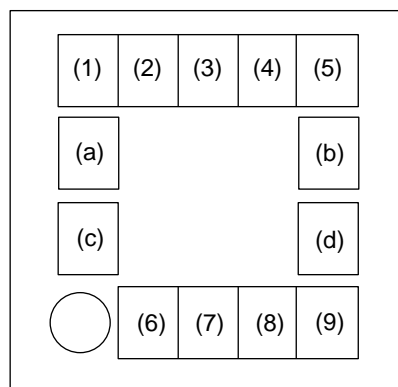
PRECAUTIONS

- All external parts should be placed as close as possible to the LNA.
- For good RF performance, all GND terminals must be connected to PCB ground plane of substrate, and via-holes for GND should be placed near the LNA.

■ MARKING SPECIFICATION

(1) (2) (3) (4) (5) (6): Product code

(7) (8) (9) (a) (b) (c) (d): Lot Number ... Alphanumeric Serial Number



DFN1616-6-GE Marking Specification

NOTICE

There can be variation in the marking when different AOI (Automated Optical Inspection) equipment is used. In the case of recognizing the marking characteristic with AOI, please contact our sales or distributor before attempting to use AOI.

DFN1616-6-GE Marking List

Product Name	(1) (2) (3) (4) (5) (6)
NT1191GEAE3A	1 1 9 1 A A

■ APPLICATION NOTES

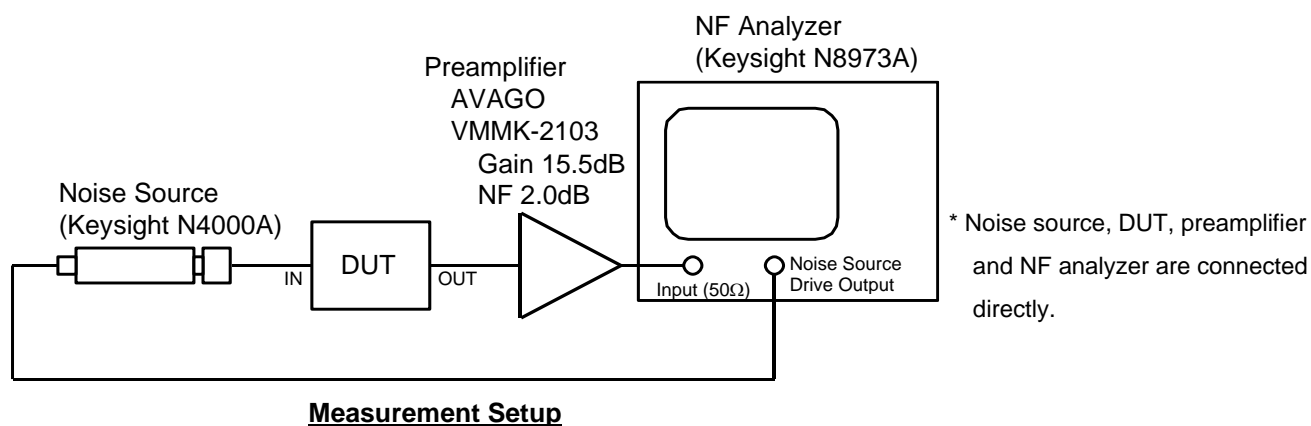
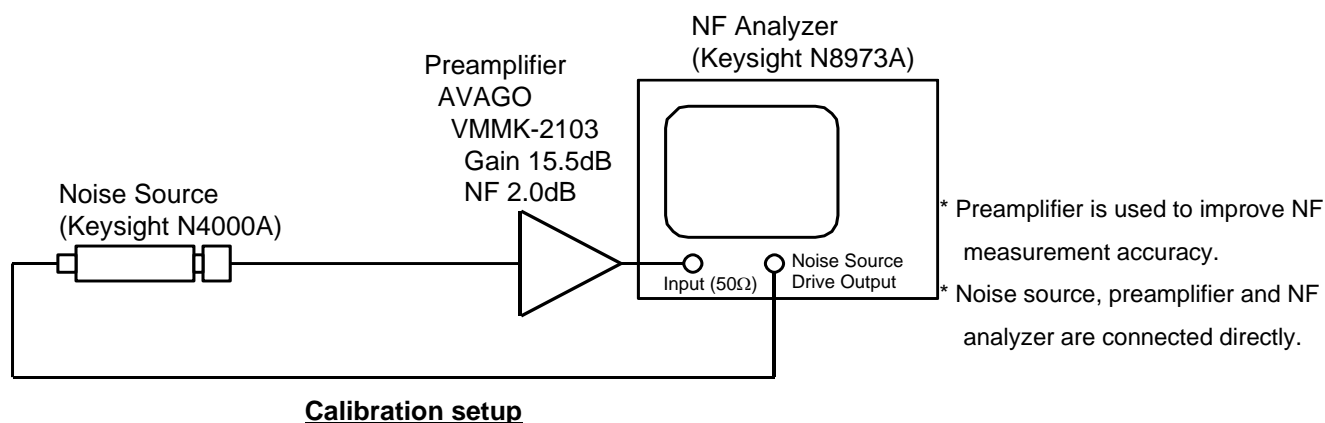
● NF Measurement Block Diagram

Measuring instruments

NF Analyzer : Keysight N8973A
Noise Source : Keysight N4000A

Setting the NF analyzer

Measurement mode form
Device under test : Amplifier
System downconverter : off
Mode setup form
Sideband : LSB
Averages : 8
Average mode : Point
Bandwidth : 4 MHz
Loss comp : off
Tcold : setting the temperature of noise source (Auto)

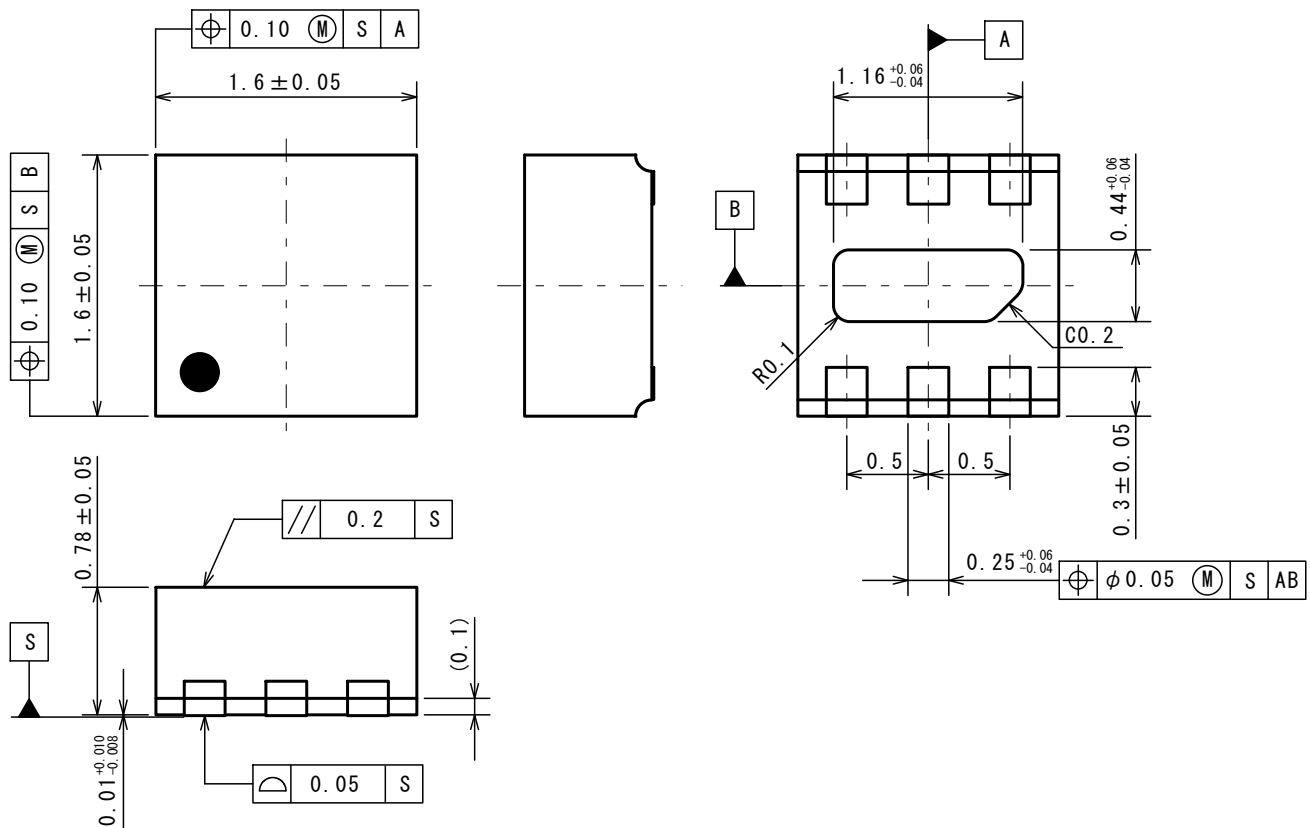


■ Revision History

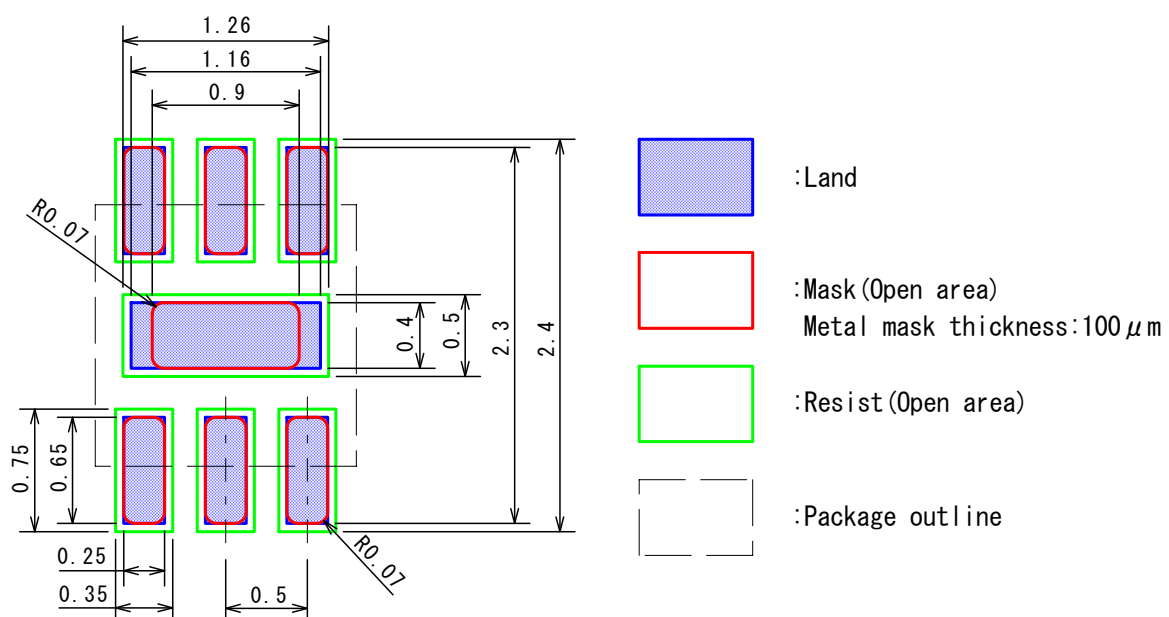
Date	Revision	Changes
November 15, 2024	Ver. 1.0	Initial release

■ PACKAGE DIMENSIONS

UNIT: mm



■ EXAMPLE OF SOLDER PADS DIMENSIONS



Nisshinbo Micro Devices Inc.

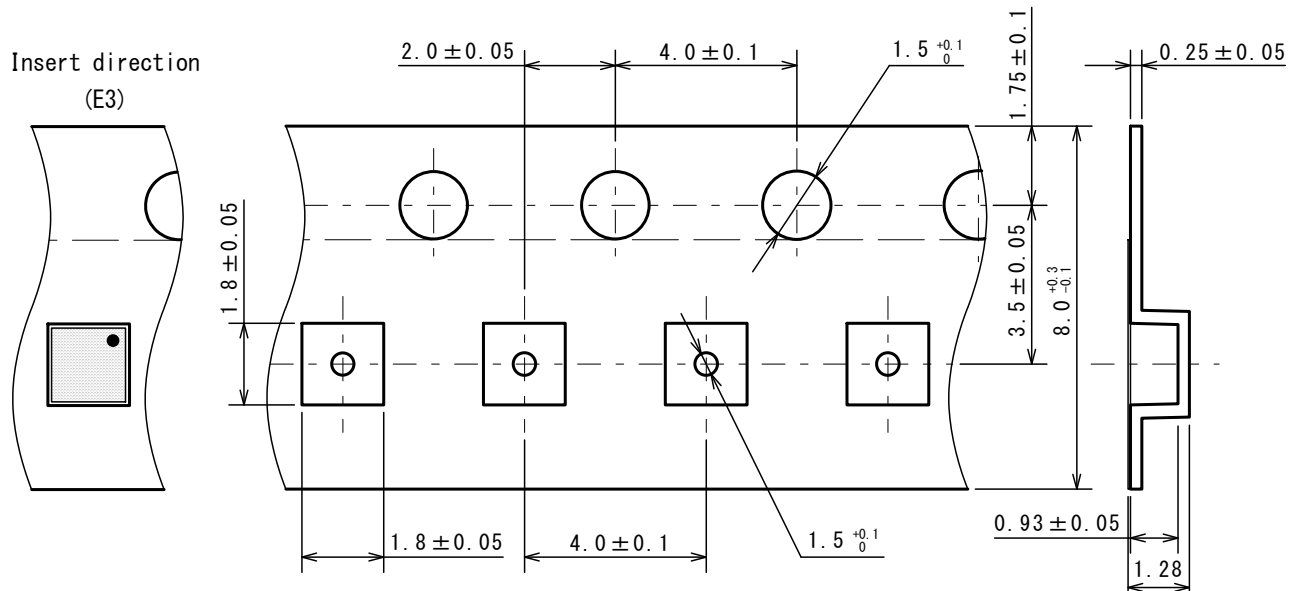
DFN1616-6-GE

PI-DFN1616-6-GE-E-B

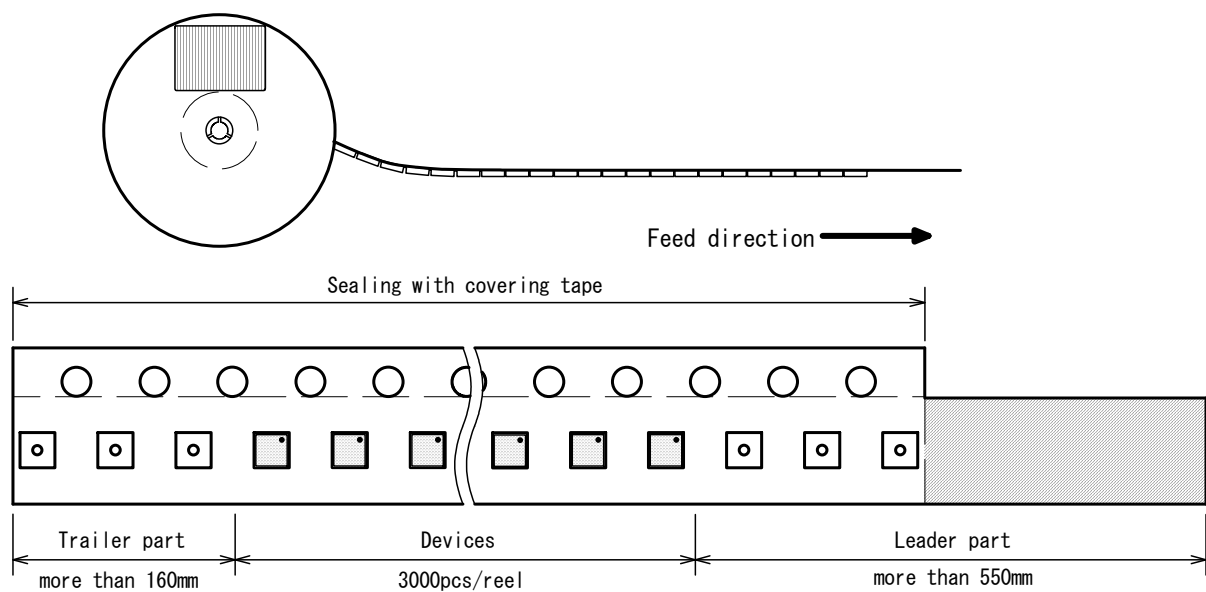
■ PACKING SPEC

UNIT: mm

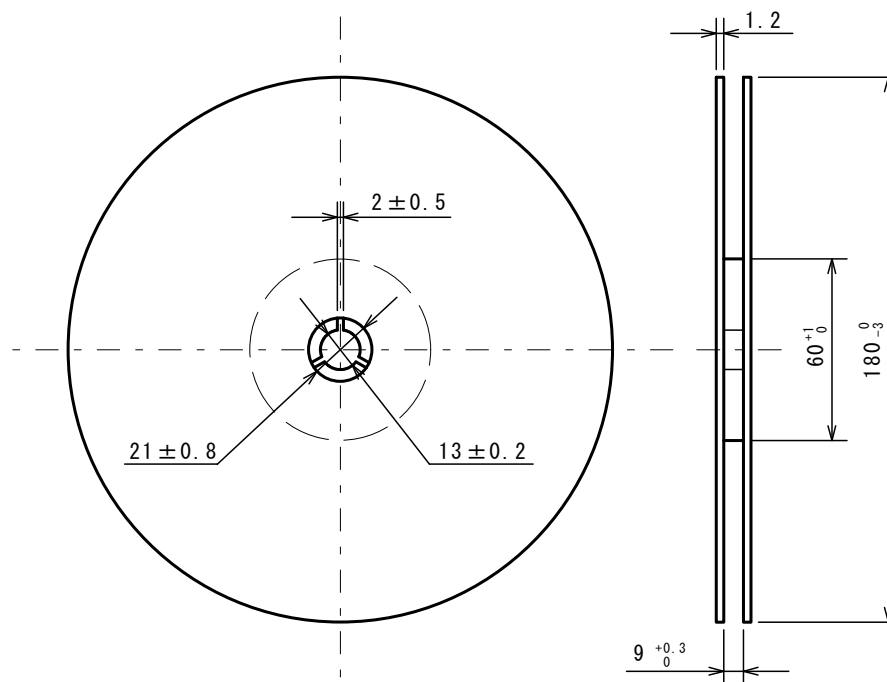
(1) Taping dimensions / Insert direction



(2) Taping state



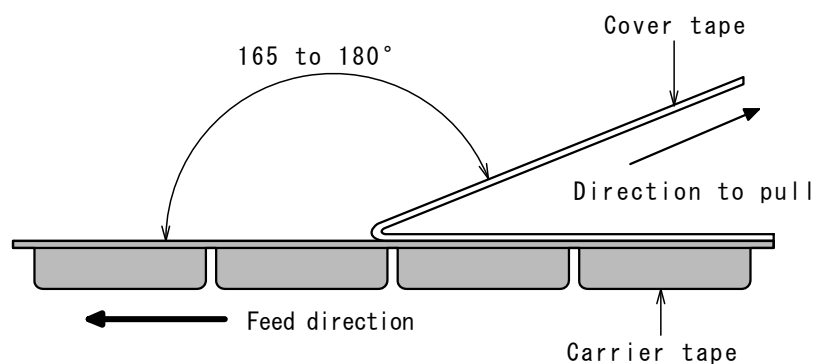
(3) Reel dimensions



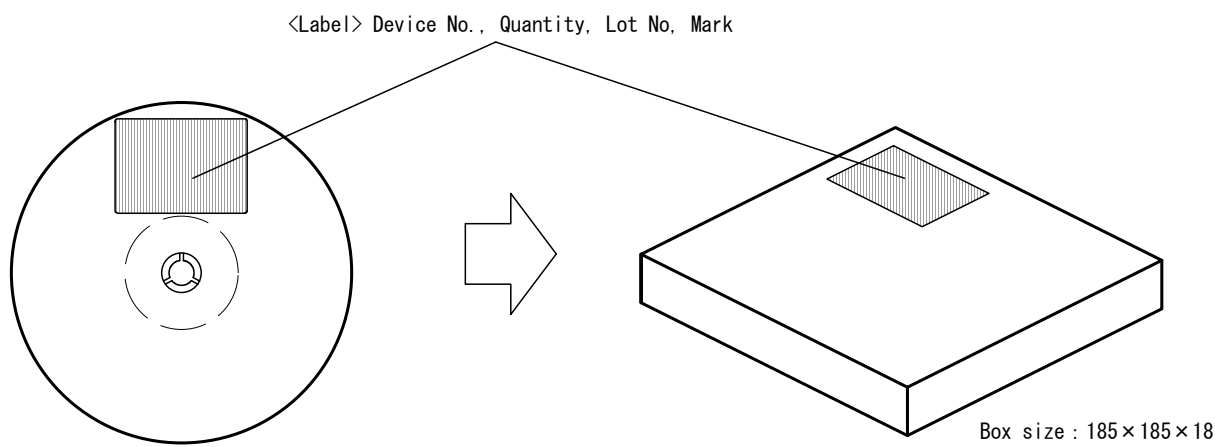
(4) Peeling strength

Peeling strength of cover tape

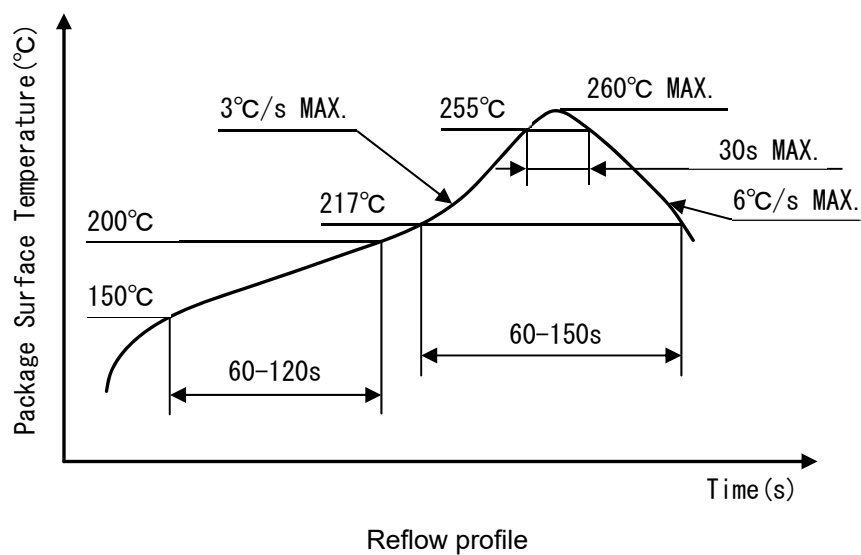
- Peeling angle 165 to 180° degrees to the taped surface.
- Peeling speed 300mm/min
- Peeling strength 0.1 to 1.0N



(5) Packing state



■ HEAT-RESISTANCE PROFILES



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 - Combustion equipment

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When it has been proved defective due to manufacturing factors as a result of defect analysis by us, we will either deliver a substitute for the defective product or refund the purchase price of the defective product.
Note that such delivery or refund is sole and exclusive remedies to your company for the defective product.
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With respect to any defect of this product found after the quality warranty period, the defect will be analyzed by us. On the basis of the defect analysis results, the scope and amounts of damage shall be determined by mutual agreement of both parties. Then we will deal with upper limit in Section 8-2. This provision is not intended to limit any legal rights of your company.
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